

Capítulo 9.

BIBLIOGRAFÍA

- 9.1 *LIBROS*
- 9.2 *ARTÍCULOS*
- 9.3 *OTROS*

9.1 LIBROS

- Phillip E. Allen, Douglas R. Holberg: **“CMOS Analog Circuit Design”**. Oxford University Press, 2002.
- David Johns, Ken Martin, **“Analog Integrated Circuit Design”**, John Wiley and Sons, Inc., 1997.
- Rudy van de Plassche, **“CMOS Integrated Analog-to-digital and digital to analog converters”**, Kluwer Academic Publishers, 2003.
- Behzad Razavi, **“Design of analog CMOS integrated circuits”**, Mc Graw Hill, 2001.

9.2 ARTÍCULOS

- Conor Donovan and Michael P. Flynn, **“A “Digital” 6-bit ADC in 0.25- μ m CMOS”**, *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 37, NO. 3, MARCH 2002.
- F. Kaess, R. Kanan, B. Hochet and M. Declercq, **“New Encoding Scheme For High-speed Flash ADC's”**, 3rd IEEE International Symposium on Circuits and Systems (ISCAS'97), Hong-Kong, pp. 5-9, June. 1997.
- R. Kanan, et al., **“A 640mW high accuracy 8-bit 1GHz flash ADC encoder”**, in *IEEE Int. Symp. Circuits and Systems*, 1999, pp. 420–423.
- C. S. Wallace, **“A Suggestion For a Fast Multiplier”**, *IEEE Trans. On Electron Computers*, pp. 1.4- 17, Feb.1964.
- Ardie G. W. Venes, Rudy J. van de Plassche, **“An 80-MHz, 80-mW, 8-b CMOS Folding A/D Converter with Distributed Track-and-Hold Preprocessing”**, *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 31, NO. 12, DECEMBER 1996, pp. 1846-1853.

9.3 OTROS

- **“A 1GSAMPLE/s 6-BIT FLASH A/D CONVERTER WITH A COMBINED CHOPPING AND AVERAGING TECHNIQUE FOR REDUCED DISTORTION IN 0.18 μ m CMOS”**, A Thesis by NIKOLAOS STEFANOU, Submitted to the Office of Graduate Studies of Texas A&M University in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE, May 2005.