1. Introduction

The first integrated circuits appeared in the early 1960s. Called "Small-Scale Integration" (SSI), the circuits contained no more than some tens of transistors and it made possible to develop the first lightweight digital computers. The next step, taken in the late 1960s, introduced devices that contained hundreds of transistors on each chip and was called "Medium-Scale Integration" (MSI). They were attractive because they allowed more complex systems to be produced using smaller circuit boards and less assembly work. Further development led to "Large-Scale Integration" (LSI) in the mid 1970s, with tens of thousands of transistors per chip. LSI circuits began to be produced in large quantities for computer memories and pocket calculators.

The final step in the development process, starting in the 1980s, was "Very Large-Scale Integration", with hundreds of thousands of transistors at the beginning, but with several millions in the latest years (ULSI, "Ultra Large-Scale Integration" is the name when the circuit contains more than 1 million of transistors, but there is no qualitative difference between VLSI and ULSI). For the first time, it became possible to fabricate a CPU on a single integrated circuit, appearing the microprocessors. Also, the first megabit RAM chips were produced.

The introduction of VLSI systems had several important consequences. One of them is that the system operation speed could be considerably increased up to few gigahertz. As semiconductor technologies operate at increasingly higher speeds, system performance has become principally limited by the ability of synchronizing the data flow signals and not only by the delay of the individual logic elements. In high-speed digital systems, clock distribution is a challenging problem that consumes an important fraction of resources and design time.

In a synchronous digital system, clock signals are used to define a time reference for the data flow within the system. This function is essential for the operation of this kind of systems. Therefore, it is fundamental to give much attention to the characteristics of the clock signal and its distribution network. System performance and reliability is directly affected by the design of the clock distribution network.

As technology sizes decrease, the delay of interconnection lines utilized in the clock distribution network increases considerably. The reason is that wire resistance is incremented substantially (smaller wire width and thickness) and, therefore, the RC wire constant. Clock skew, the difference between clock signal arrival times to two sequentially adjacent registers, is directly related to the clock path delay. A higher path delay causes a higher clock skew between these paths.

Clock skew is a key challenge for high-speed circuit designers because it can degrade performance and cause chip failures. There is a designer's rule of thumb that imposes that clock skew must be lower than the 10% of the clock period. As clock frequency goes up, better clock distribution networks are required to keep skew at a constant fraction of the cycle time. The growing die size, clock loads and process variability aggravate the problem. Even when clock skew is completely designed to be zero, environmental and processing variations lead to significant amounts of skew.

At first, the motivation of this work is to give a general overview of the different existent solutions for the implementation of a clock distribution system. Their main parameters and design techniques will be presented. Theoretical background and sources of clock skew are described. The main goal is to analyse the different existent models for estimating the clock skew according to all technology parameters. They are compared for a generic global clock distribution network (an H-tree). Simulations are done with a JAVA program developed to calculate the clock skew according to each model equations. At the end, a prevision for the clock skew value in next years will be given thanks to the use of these models.

This work is organized in the following parts:

- In section 2, a general overview of clock distribution networks is presented. Firstly, synchronous digital systems are described and also the function of a clock distribution network within them. Main strategies of design are presented, starting with the buffered trees and all their possible topologies. Primary parameters of a clock distribution network are introduced because they determine how the clock system should be designed. At the end of this section,

some examples of the clocking issue in commercial digital system are explained.

- In section 3, clock skew is investigated in depth. At first, a theoretical background of the clock skew is presented. Secondly, all possible causes of clock skew (process and circuit parameter variations) are introduced. The third part of this section is one of the most important of the work. Existent clock skew models are described and their equations to calculate clock skew estimations are presented.

- In section 4, the main goal of the work is described. Clock skew models are compared for a specific global clock distribution network (a 256 nodes H-tree, 130 nm technology) that is designed according to some optimization methods (optimal wire and buffer sizes). Different simulations are made with a JAVA program. The results are analysed. At the end, the same simulations are made but with the predicted technology parameters for the future.

- Finally, in section 5, the conclusions of this work are presented.