4. Comparison between clock skew models

The main goal of this work is to analyse the existent clock skew models and to determine which gives us the most accurate clock skew estimation for a specific clock distribution network. The efficiency of these models is going to be studied applying them to a generic H-tree structure, which is often used in the global part of a clock distribution network (higher hierarchical level).

At first, in section 4.1, a specific design methodology is presented. An H-tree with optimized buffers and wire sizes is going to be implemented. In the next section 4.2, the technology parameters of the 130 nm technology are shown in different tables. In section 4.3, numerical results of the simulations are presented. They have been done thanks to the JAVA program *"equations"*. This program calculates clock skew estimations according to the equations of the three analysed models. In appendix 4, program operation is presented. Finally, in section 4.4, clock skew estimations for future technologies are presented.

4.1. Design methodology

There are different possibilities for the structure of an H-tree clock distribution network. There could be intermediate buffers at the branching points (models 1 and 3) or not (model 2). In the second case, wire widths must be widened to avoid signal reflections at these split points.

In this work, the H-tree utilized for models simulations is going to be designed optimizing their buffers and wire sizes (width, thickness and length) according to different optimization methods. The result of optimizing interconnection length is that if in any level of the H-tree any branch length is longer than the optimal length, it is divided in k sections inserting optimal size inverters. The topology resultant is illustrated in the following figure 4.1:

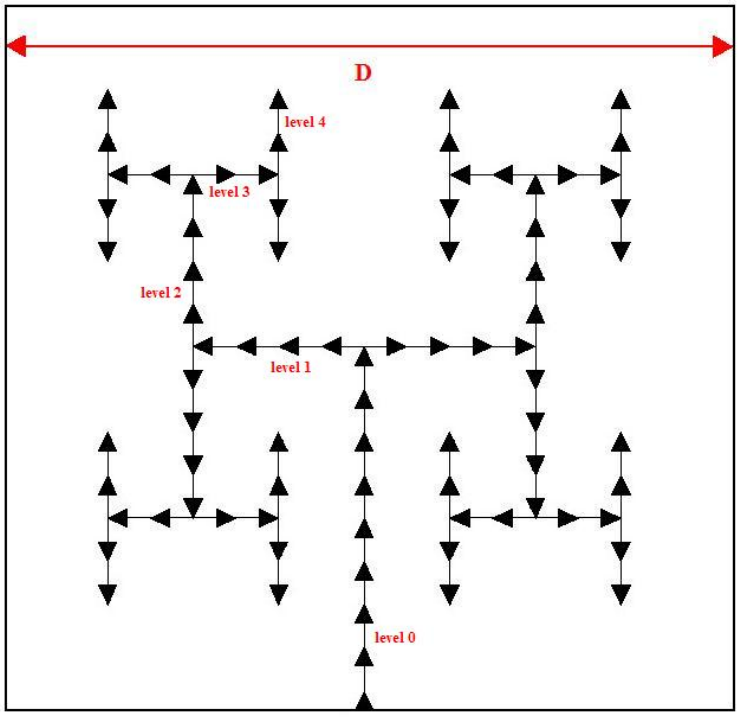

Figure 4.1: Buffered H-tree with optimized wire dimensions.

The first step is to characterize interconnection wires. Azad Naeemi, Raguraman Venkatesan and James D. Meindl present two methods (RC wire model and RLC wire model) [NAE-01], [NAE-02] where wire width is optimized for any technology. Since the inductance starts to become significant for long metal interconnections and high frequency operation, the RLC method has been chosen in this work. The optimal wire width is given by this expression:

$$W_{opt} = 1.88 c_0 \sqrt{\xi \rho \varepsilon_0 R_0 C_0} \qquad (4.1)$$

where c_0 is the speed of light in vacuum, ξ a constant depending on the wire geometry, ρ the metal resistivity, ε_0 the dielectric constant in vacuum, and R_0 and C_0 the output resistance and input capacitance of the minimum size repeater. For such interconnect width, wire thickness is calculated according the technology aspect ratio parameter. Then, using analytical models and formulas, the resistance, capacitance and inductance for wires are calculated.

The next step is to determine the optimum number and buffer size that we are going to insert in the H-tree. In this way, dividing branches in optimal length sections, their delay time is minimized [ISM-00]. If this time is smaller, then the clock skew is also smaller (because clock skew depends on the standard deviation of the path delay). The equivalent resultant wire after being divided is shown in figure 4.2:

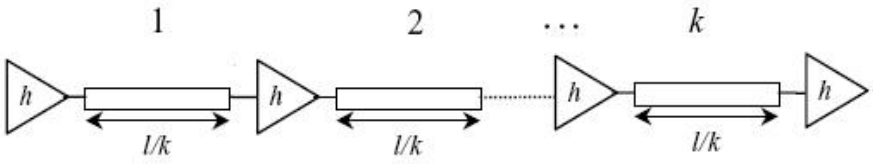

Figure 4.2: Repeaters inserted in an *RLC* line to minimize the propagation delay.

Now time expressions are transformed in the next ones:

$$T_{delay} = k \cdot T_{segment}$$
$$T_{segment} = 2.3\frac{R_0}{h}\left(\frac{C_{\text{int}}}{k} + hC_0\right) + \frac{R_{\text{int}}}{k}\left(\frac{C_{\text{int}}}{k} + 2.3hC_0\right) \qquad (4.2)$$

where $T_{segment}$ is the delay per line segment, C_0 and R_0 are the input capacitance and output resistance of the minimum size inverter, C_{int} and R_{int} are the capacitance and resistance of the interconnection line in the path, k is the number of segments and h is the number of times that the inverters are bigger than the minimum size inverter. According to the expressions presented in [ISM-00], the optimal values of k and h taking into account the inductive wire effects are:

$$h_{opt} = \sqrt{\frac{R_0 C_{int}}{R_{int} C_0}} \frac{1}{\left[1 + 0.16\left(T_{L/R}\right)^3\right]^{0.24}} \qquad (4.3)$$

$$k_{opt} = \sqrt{\frac{R_{\text{int}} C_{int}}{2R_0 C_0}} \frac{1}{\left[1 + 0.18\left(T_{L/R}\right)^3\right]^{0.3}} \qquad (4.4)$$

where $T_{L/R}$ is:

$$T_{L/R} = \sqrt{\frac{L_{\text{int}} / R_{int}}{R_0 C_0}} \qquad (4.5)$$

In those expressions, R_{int}, L_{int} and C_{int} are the total resistance, inductance and capacitance of the line.

By other hand, in VLSI circuits, clocks lines are usually shielded by ground and power lines to reduce the noise coupled into signal lines from the clock lines. Furthermore, in this way the modelling of the capacitive and inductive wire characteristics is easier, resulting predictable equations that allow control the delay of each clock signal path and the clock skew between them.

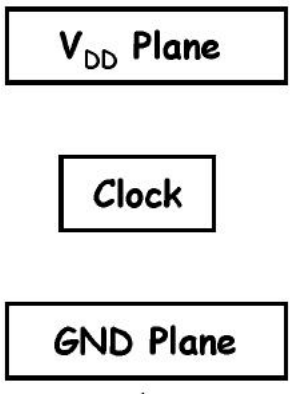

Figure 4.3: Wiring structure.

Models 1 and 3 can be applied to same clock distribution network topology: An H-tree with intermediate buffers at split points and same wire width at each level of the tree. Model 2 is applied to the other H-tree possibility, a tapered H-tree without intermediate buffers and widened wire widths. Therefore, some changes have to be done to compare the results of that model with the other two models results.

- Model 2 differences

The main difference in the equations of this model, comparing to models 1 and 3, is the parameter $r_{int}c_{int}$. It is the distributed capacitance and resistance of the line from the root to the leaf because no buffer is placed between them.

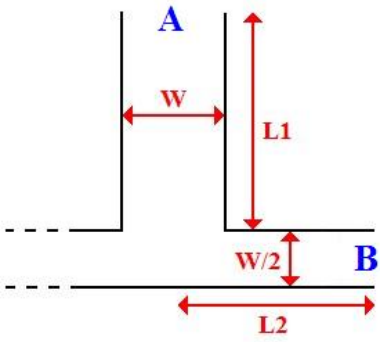

Figure 4.4: Wire diagram in model 2.

In an H-tree, wire width is doubled at each higher lever. In figure 4.4, the parameters of a tapered section are shown. The total resistance and capacitance from point A to point B are:

$$\begin{aligned} r_1 c_1 &= rc \\ r_2 c_2 &= 2r \cdot \frac{c}{2} = rc \\ RC_{total} &= rc \cdot \left(L_1 + L_2\right)^2 \end{aligned} \qquad (4.6)$$

where r and c are the resistance and capacitance per wire length unit. We can see that parameter $r_{int}c_{int}$ is the same in each level of the clock H-tree. It is a constant value. Therefore, in model 2, to calculate $r_{int}c_{int}$, we only have to multiply the parameters R_{int} and C_{int} of the models 1 and 3.

The parameter C_L in the model 2 equations is the capacitive load of the following sub-block in the hierarchical clock distribution network. We are going to assume that it is the input capacitance of the buffer that drives the next level sub-block, so we can use the same C_0 that we have in models 1 and 3. According to model 2 equations, the variance of C_L is going to be assumed 0 because we decided before that C_L is input capacitance of a buffer, so with the variance of V_t, t_{ox}, L_{eff} and V_{dd} the variance of C_L is defined.

The resultant tapered H-tree structure is shown in picture 4.5. The lowest level wire width is the minimal and it doubles at each higher level. No intermediate buffers are placed at split points.

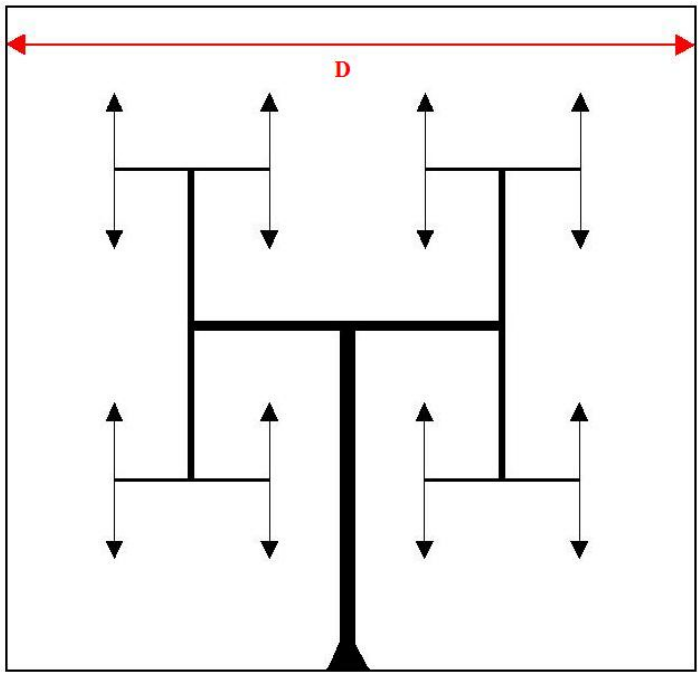

Figure 4.5: Tapered H-tree.

4.2.H-tree parameters (technology parameters)

In this section, the parameters of the 8 levels H-tree that is going to be utilized in simulations are presented. The chosen technology is 130 nm. Parameters are extracted from the ITRS roadmap and from the result of applying the design methodology equations. The first table shows the primary parameter of the 130 nm technology, like CMOS device parameters and minimal size interconnection wire parameters.

Parameter	Description	Value
V_{DD}	Supply voltage	1.2 V
V_T	Threshold voltage	0.19 V
T_{ox}	Gate oxide thickness	3.3 nm
D	Die size	17.32 mm

ε_{ILD}	Dielectric constant (interlevel)	3.6
W_{int} (min)	Minimal wire width	335 nm
A/R	Wire aspect ratio (t_{int} / W_{int})	2
t_{int} (min)	Minimal wire thickness	670 nm
R_0 (min)	Buffer output resistance (min. size inv.)	3.94 kΩ
C_0 (min)	Buffer input capacitance (min. size inv.)	0.77 fF

Table 4.1: 130 nm technology parameters [ITRS].

After applying the formulas to calculate optimized buffers and wire dimensions, next table shows buffer and wire parameters that are going to be used in the simulations.

Parameter	Description	Value
W_{int} (opt)	Optimal wire width	1250 nm
t_{int} (opt)	Optimal wire thickness	2500 nm
L_{int} (opt)	Optimal segment length	2.88 mm
W (opt)	Optimal buffer size (optimal width)	322 μm

Table 4.2: Optimized parameters.

The following table shows the number of required buffers in an 8 levels H-tree according to the optimal wire partition and the die size of the 130 nm technology.

Level	Branch length	Required buffers
0	D/2 = 8.66 mm	3
1	D/4 = 4.33 mm	2
2	D/4 = 4.33 mm	2
3	D/8 = 2.17 mm	1
4	D/8 = 2.17 mm	1
5	D/16 = 1.08 mm	1
6	D/16 = 1.08 mm	1
7	D/32 = 0.54 mm	1
8	D/32 = 0.54 mm	1

Table 4.3: Required buffers at each level.

Finally, next table shows the definitive parameters of the clock distribution network that is going to be utilized in the simulations. It is an 8 levels H-tree with optimized buffers and wire dimensions.

Parameter	Description	Value
N	Number of nodes	256
D	Chip size	17.32 mm
R_{int}	Interconnection resistance (optimal)	7.04e3 Ω/m
C_{int}	Interconnection capacitance (optimal)	3.4e-10 F/m
$C_{w\text{-}total}$	Total wire capacitance (397.76 mm)	135.24 nF
R_0	Buffer output resistance (optimal)	1.59 Ω
C_0	Buffer input capacitance (optimal)	1.91e-12 F
$C_{b\text{-}total}$	Total buffer capacitance (775 buffers)	1.48 nF

Table 4.4: H-tree parameters.

Finally, in the last table, process and circuit parameter tolerances are shown. It is necessary to know them because they are the input parameters of the JAVA program for the simulations. The transistor width deviation is calculated according to the minimal size technology deviation. It means that the value given for the 130 nm technology is referred to the minimum size transistor lithography. For optimal size transistors, the absolute value of the deviation is the same. Consequently, the percentage of deviation is smaller. The same calculations are done for the optimal wire width and thickness according to the deviation of minimal size wires.

Parameter	Description	Standard Deviation
σ_{VDD}	Power supply voltage	3.3 % [KAH-01]
σ_{VT}	Threshold voltage	4.2 % [KAH-01]
σ_{μ}	Charge carrier mobility	2 % [KAH-01]
σ_{tox}	Gate oxide thickness	1.3 % [KAH-01]
σ_{W}	Transistor width	5% of 130 nm → [KAH-01] 2.02e-3 % of 322 μm
σ_{Leff}	Transistor effective channel length	5 % [KAH-01]
σ_{Wint}	Wire width	3% of 335 nm → [FAN-98] 0.804% of 1250 nm
σ_{tint}	Wire thickness	3% of 670 nm → [FAN-98] 0.804% of 2500 nm
σ_{TILD}	ILD thickness	3 % [FAN-98]
σ_{T}	Temperature	8% [GRO-98]

Table 4.5: Parameter tolerances.

As was said in the previous section, model 2 requires some different parameters. First of them is $r_{int}c_{int}$, the distributed capacitance and resistance of the line from the root to the leaves. It is calculated multiplying the same optimal R_{int} and C_{int} that were used in models 1 and 3. C_L is the same input capacitance than C_0 in the previous models. Wire width variation σ_{Wint} is calculated for the worst case (last level width = optimal width).

Parameter	Description	Value
$\mathbf{r_{int}c_{int}}$	Distributed capacitance and resistance	2.39e-6 s/m^2
$\mathbf{C_L}$	Load capacitance	1.91e-12 F

Table 4.6: Model 2 parameter differences.

4.3. Simulations

To analyse the different clock skew models with the proposed H-tree described in the previous section (256 nodes, 130 nm technology), three different simulations have been realised. In the first of them, the value of the clock skew according to each model is compared. Secondly, each clock skew component is individually analysed to determine with parameter deviation has higher influence on the total clock skew value. The third simulation shows the clock skew estimation for different number of H-tree end points (number of levels).

We have to take into account that each model considers different clock skew sources. For example, only model 2 considers the temperature variation, or moreover the case that model 3 considers transistor width variations but model 1 does not.

4.3.1. First simulation

Clock skew estimations for the three models in a 256 nodes H-tree and 130 nm technology.

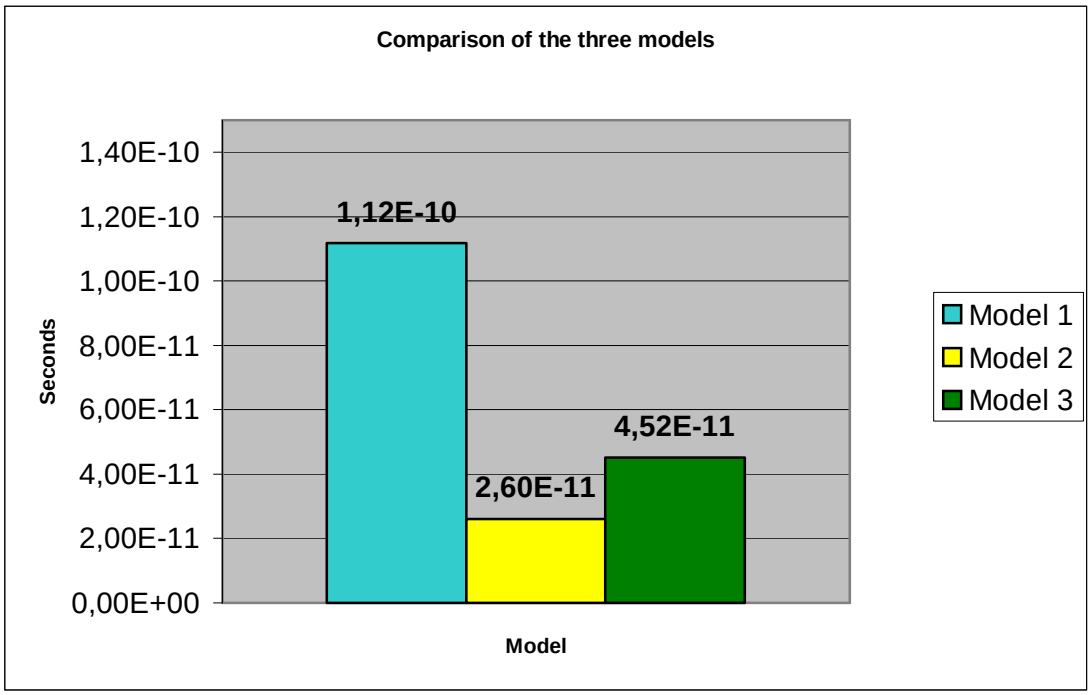

Figure 4.6: Clock skew estimations according to each model.

We can observe that the results are the expected. Model 1 gives us a value of *112 ps* for an H-tree with intermediate buffers and model 3 gives a value of *45.2 ps*. It is correct because the first model estimates an upper bound for the clock skew and the third model calculates the clock skew more accurately since it takes into account the correlation between overlapped parts of clock paths. Model 2 estimation is realized with a different clock distribution network topology, a tapered H-tree without intermediate buffers. The value of *26 ps* is accepted because it must be smaller than the values for buffered H-trees, where more sources of clock skew are present along the paths (intermediate buffers). The reliability of these estimations depends on how accurately the clock system parameters have been predicted.

4.3.2. Second simulation

Clock skew components according to each model in a 256 nodes H-tree and 130 nm technology.

- MODEL 1

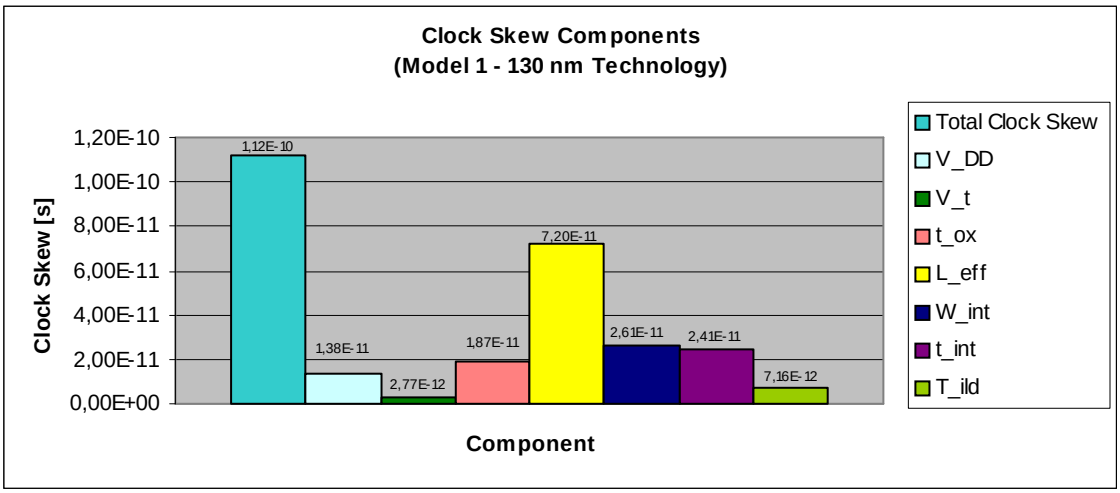

Figure 4.7: Components of the clock skew in model 1.

According to model 1 (and the parameter tolerance predictions), an important conclusion can be drawn: the tolerance of L_{eff}, the effective channel length, should be specially controlled because it is the main source in the total clock skew. The influence of this parameter (tolerance of *5 %*) is higher compared to the gate oxide thickness, t_{ox}, another transistor source of skew, but with smaller tolerance (*1.3 %*). As it was said in previous sections, buffers are the main source of clock skew. Their parameters may be accurately controlled to obtain low skew H-trees. Wire sources of skew are less important if their tolerances are not particularly significant.

- MODEL 2

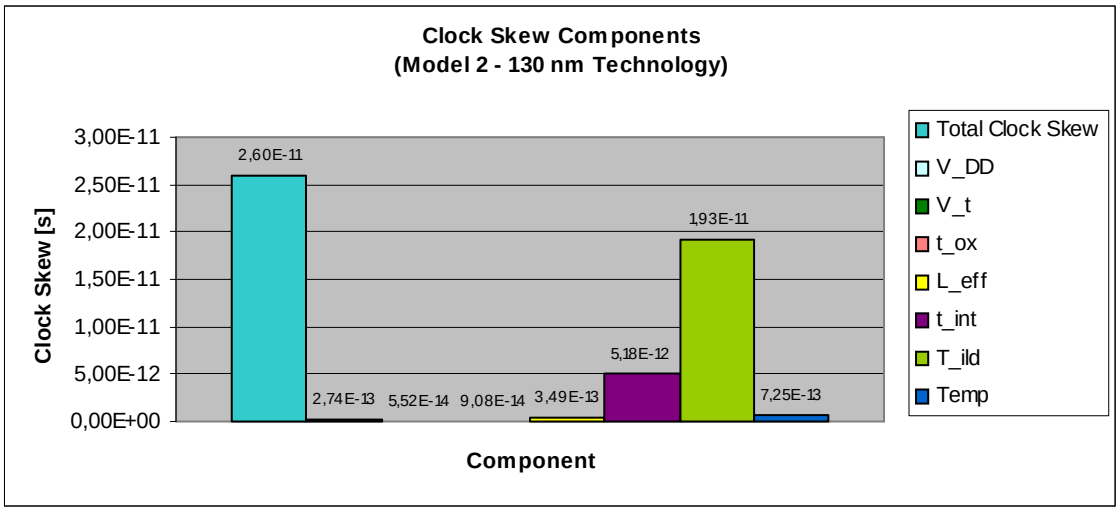

Figure 4.8: Components of the clock skew in model 2.

The main conclusion that can be extracted after simulate the model 2 in a tapered H-tree is that wire clock skew sources are more important than buffer sources. It is consequent because a tapered H-tree with *256* nodes has only *257* buffers and the optimized H-tree utilized in models 1 and 3 simulations has *576* buffers. By other hand, the ILD thickness is the main source among wire skew sources. It is due to a higher variance (*3 %)* than wire thickness variation (*0.804 %*).

- MODEL 3

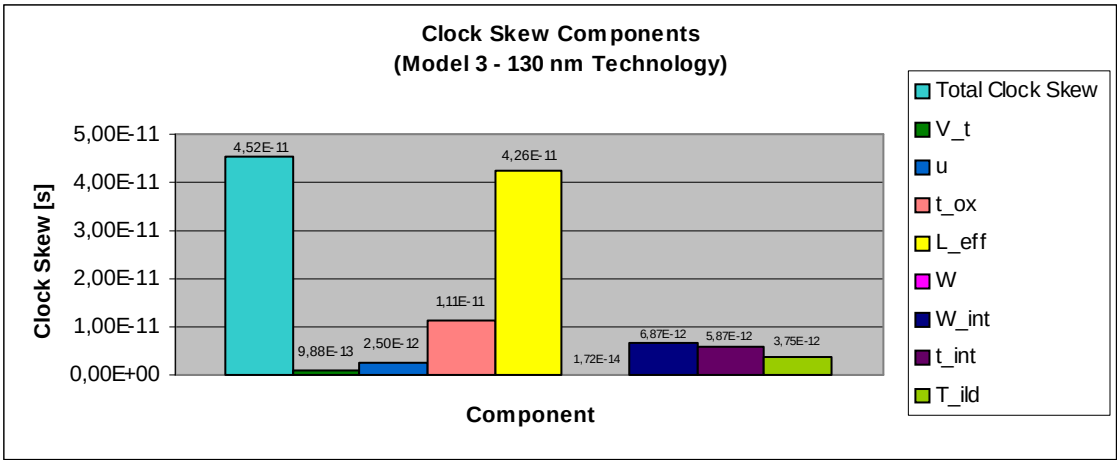

Figure 4.9: Components of the clock skew in model 3.

Practically the same conclusions than were drawn for the first model simulation can be drawn. Buffers parameters, principally L_{eff}, are the main source of clock skew. A different parameter, which model 1 does not consider, is transistor width *W*. The effect of it is almost negligible due to the very low tolerance value of this parameter (*2.02e-3 %*).

4.3.3. Third simulation

Clock skew estimations for different number of nodes in an H-tree implemented in the 130 nm technology.

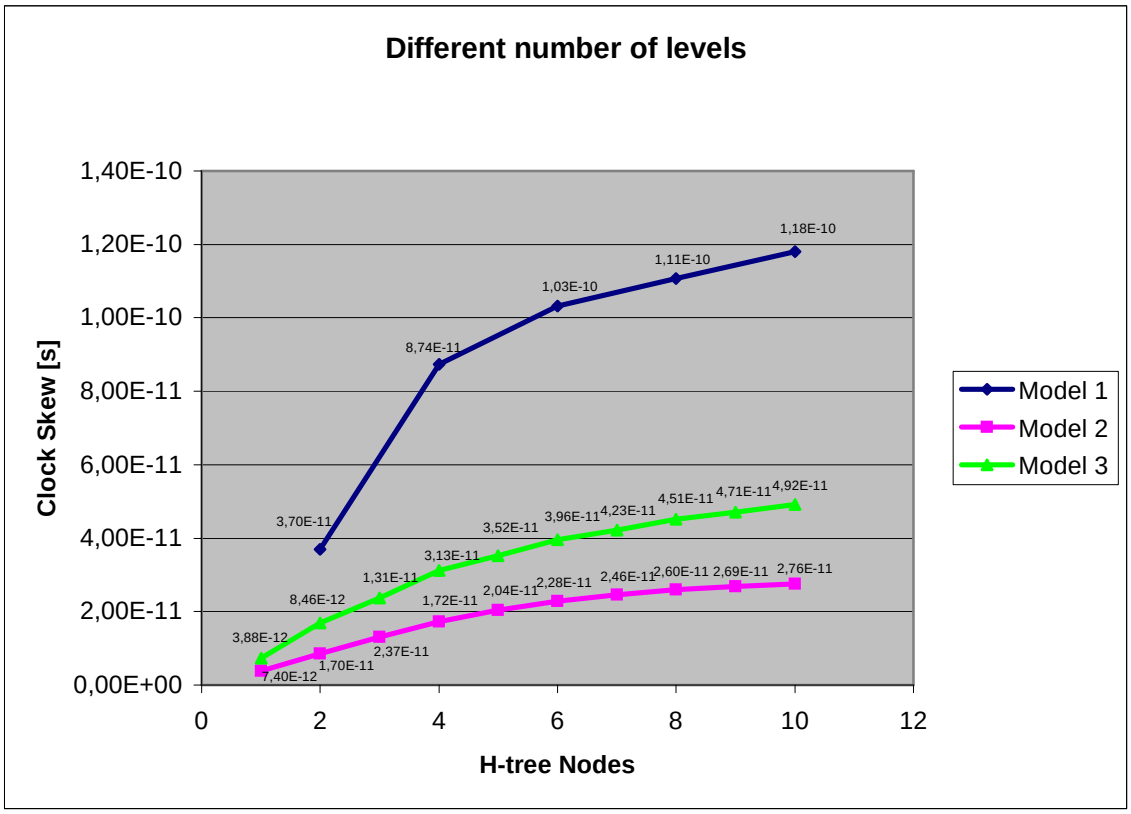

Figure 4.10: Clock skew in the 130 nm technology for different number of levels.

The results are again the expected. In every case, the clock skew value given by the model 3 is lower than the given by the model 1. It is logical because model 1 only provides an upper bound for the clock skew. Model 3 gives us a value considering the correlation between paths, so the value is less conservative. Estimations for model 2 are always the smallest. It is because the tapered H-tree has less clock skew sources than the equivalent optimized buffered H-tree.

We can observe how the clock skew increase as number of levels in the H-tree is bigger. This increase is less appreciable for high number of levels because when we add a new one, we are just adding a new buffer and a very small interconnection section.

On the other hand, model 1 estimations are made only for a even number of levels. Their equations have no meaning when they are applied to H-trees with an odd number of levels.

4.4. Clock skew for future technologies

Once the three models have been analysed and simulated, and several conclusions about them have been drawn, it is possible to apply them to a global clock distribution network designed with future technology parameters: an 8 levels H-tree implemented in 100, 70 and 45 nm technologies. We can verify how the clock skew will be in the future for this topology and if an H-tree like that will be appropriate within a global clock distribution network.

At first, technology parameters of these technologies are presented in the following table. We can compare them to the 130 nm parameters.

Parameter	130 nm	100 nm	70 nm	45 nm
V_{DD}	1.2 V	1 V	0.9 V	0.6 V
V_T	0.19 V	0.15	0.06	0.021
T_{ox}	3.3 nm	2.5 nm	1.6 nm	1.4 nm
D	17.32 mm	17.32 mm	20 mm	21.21 mm
ε_{ILD}	3.6	3.3	3	3.6
W_{int} (min)	335 nm	237 nm	160 nm	103 nm
A/R	2	2.1	2.2	2.3
t_{int} (min)	670 nm	500 nm	352 nm	235 nm
R_0 (min)	3.94 kΩ	4.95 kΩ	8.02 kΩ	15.7 kΩ
C_0 (min)	0.77 fF	0.66 fF	0.457 fF	0.34 fF

Table 4.7: Technology parameters for the chosen technologies [ITRS].

After applying the equations, the optimized parameters for the buffer and wire size are in the next table:

Parameter	130 nm	100 nm	70 nm	45 nm
W_{int} (opt)	1250 nm	1005 nm	850 nm	620 nm
t_{int} (opt)	2500 nm	2110 nm	1870 nm	1426 nm
L_{int} (opt)	2.88 mm	2.16 mm	1.67 mm	1.32 mm
W (opt)	322 µm	354 µm	496 µm	648 µm

Table 4.8: Optimized parameters.

The following table shows the number of required buffers in a 256 nodes H-tree according to the optimal segment partition and the die size in the 130 nm technology.

		130 nm		100 nm		70 nm		45 nm	
Level	**Section**	**Length**	**Buffs.**	**Length**	**Buffs.**	**Length**	**Buffs.**	**Length**	**Buffs.**
0	D/2	8.66mm	3	8.66mm	4	10mm	6	10.6mm	8
1	D/4	4.33mm	2	4.33mm	2	5mm	3	5.30mm	4
2	D/4	4.33mm	2	4.33mm	2	5mm	3	5.30mm	4
3	D/8	2.17mm	1	2.17mm	1	2.5mm	2	2.65mm	2
4	D/8	2.17mm	1	2.17mm	1	2.5mm	2	2.65mm	2
5	D/16	1.08mm	1	1.08mm	1	1.25mm	1	1.33mm	1
6	D/16	1.08mm	1	1.08mm	1	1.25mm	1	1.33mm	1
7	D/32	0.54mm	1	0.54mm	1	0.63mm	1	0.67mm	1
8	D/32	0.54mm	1	0.54mm	1	0.63mm	1	0.67mm	1

Table 4.9: Required buffers at each level.

Finally, next table shows the definitive parameters of the clock distribution network that is going to be utilized in the simulations. It is a 8 level H-tree (256 nodes) with optimized buffers and wire dimensions.

Parameter	**130 nm**	**100 nm**	**70 nm**	**45 nm**
N	256	256	256	256
D	17.32 mm	17.32 mm	20 mm	21.21 mm
R_{int}	7.04e3 Ω/m	10.04e3 Ω/m	13.8e3 Ω/m	24.9e3 Ω/m
C_{int}	3.4e-10 F/m	3.11e-10 F/m	2.92e-10 F/m	2.64e-10 F/m
$C_{w\text{-}total}$	135.24 nF	123.70 nF	134.32 nF	128.73 nF
R_0	1.59 Ω	1.40 Ω	1.13 Ω	1.09 Ω
C_0	1.91e-12 F	2.34e-12 F	3.24e-12 F	4.90e-12 F
$C_{b\text{-}total}$	1.48 nF	1.82 nF	2.62 nF	4.00 nF

Table 4.10: H-tree parameters.

One of the biggest problems presented during the elaboration of this work was the difficulty in searching the exact parameters for different technologies. Due to this reason, tolerances of the required parameters are going to be chosen the same than the 130 nm case. Therefore, the following table presents them.

Par.	130 nm	100 nm	70 nm	45 nm
σ_{VDD}	3.3 % [KAH-01]	3.3 % [KAH-01]	3.3 % [KAH-01]	3.3 % [KAH-01]
σ_{VT}	4.2 % [KAH-01]	4.2 % [KAH-01]	4.2 % [KAH-01]	4.2 % [KAH-01]
σ_{μ}	2 % [KAH-01]	2 % [KAH-01]	2 % [KAH-01]	2 % [KAH-01]
σ_{tox}	1.3 % [KAH-01]	1.3 % [KAH-01]	1.3 % [KAH-01]	1.3 % [KAH-01]
σ_{W}	5% of 130 nm → 2.02e-3 % of 322 µm [KAH-01]	5% of 130 nm → 2.02e-3 % of 322 µm [KAH-01]	5% of 130 nm → 2.02e-3 % of 322 µm [KAH-01]	5% of 130 nm → 2.02e-3 % of 322 µm [KAH-01]
σ_{Leff}	5 % [KAH-01]	5 % [KAH-01]	5 % [KAH-01]	5 % [KAH-01]
σ_{Wint}	3% of 335 nm → 0.804% of 1250 nm [FAN-98]	3% of 237 nm → 0.707% of 1005 nm [FAN-98]	3% of 160 nm → 0.565% of 850 nm [FAN-98]	3% of 103 nm → 0.498% of 620 nm [FAN-98]
σ_{tint}	3% of 670 nm → 0.804% of 2500 nm [FAN-98]	3% of 670 nm → 0.711% of 2110 nm [FAN-98]	3% of 352 nm → 0.565% of 1870 nm [FAN-98]	3% of 235 nm → 0.494% of 1426 nm [FAN-98]
σ_{TILD}	3 % [FAN-98]	3 % [FAN-98]	3 % [FAN-98]	3 % [FAN-98]
σ_{T}	8% [GRO-98]	8% [GRO-98]	8% [GRO-98]	8% [GRO-98]

Table 4.11: Parameter tolerances.

The next figure 4.11 shows the estimation for the 256 nodes H-tree (8 levels) designed according to four different technologies: 130 nm, 100 nm, 70 nm and 45 nm.

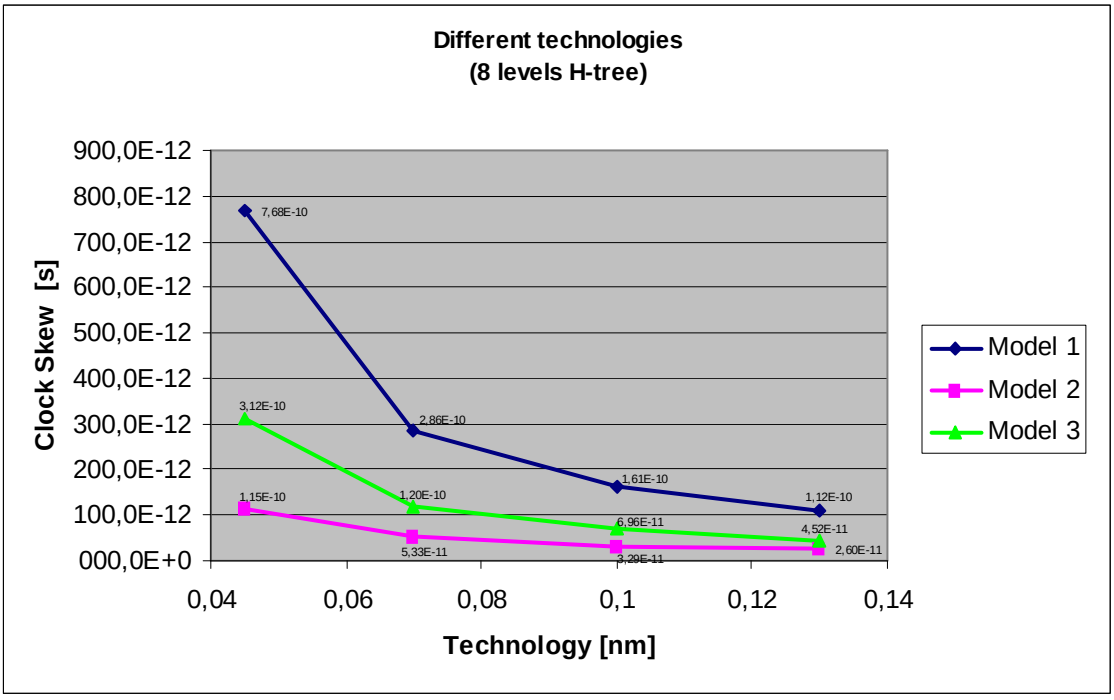

Figure 4.11: Clock skew for different technologies (130, 100, 70, 45 nm).

In every case, the clock skew value given by model 3 is lower than the given by model 1. It is logical because model 1 only provides an upper bound for the clock skew. Model 3 gives us a value considering the correlation between paths, so the value is less conservative. Model 2 estimations for the tapered H-tree are always smaller than the estimations for the H-tree with intermediate buffers. It is reasonable because there are less clock skew sources in a tapered H-tree (less buffers).

On other hand, an increasingly clock skew is observed as technology size is decreasing. It is due to the increase of the RC constant (both wires and inverters) when technology size decreases. The raise is exponential, so for each new technology the clock skew in an H-tree increases considerably. That presents a big problem because one of the main goals of a newer technology is to achieve higher clock frequencies. To do that, clock skew has to be kept proportional to the clock period (10 % approximately). In the next table and in figure 4.12, the relation between the clock skew and the clock period is shown. Only an H-tree implemented in the 130 nm technology can satisfy the design rule of 10 %.

Parameter	130 nm	100 nm	70 nm	45 nm
Clock frequency [ITRS]	1.6 GHz	3.0 GHz	9 GHz	15 GHz
Clock period	625 ps	333 ps	111 ps	66.7 ps
Clock skew (model 3)	45.2 ps	69.6 ps	120 ps	312 ps
% (Clock skew vs. period)	6.8 %	20.9%	108.1 %	467.8 %

Table 4.12: Relation between clock skew and clock period.

An important conclusion can be drawn from this simulation: a single H-tree like that is not appropriate if we want small clock skew values for a global clock distribution network. Additional methods like deskew circuits or feedbacks are necessary to obtain low skew clock distribution networks in modern technologies.

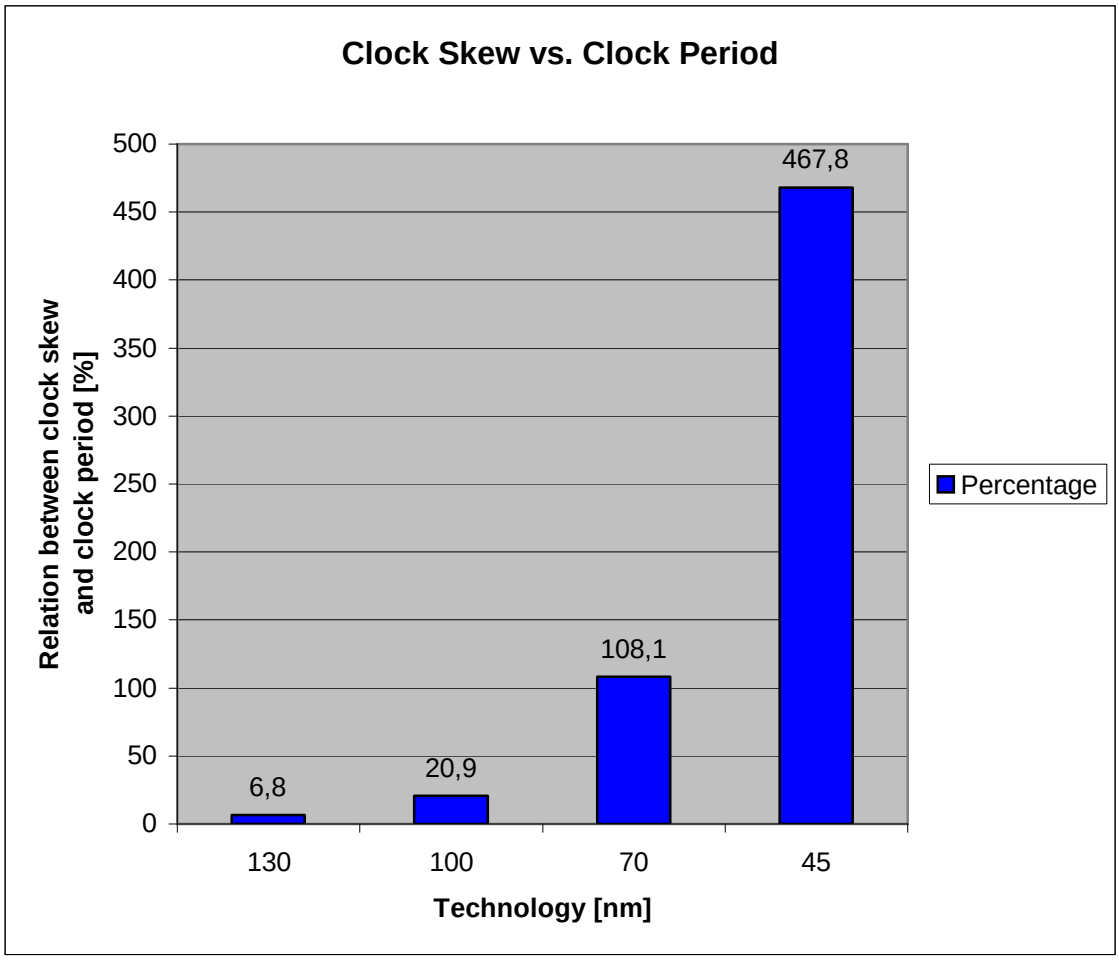

Figure 4.12: Clock skew vs. Clock period.