5. Conclusions

In this work several aspects about the clock skew within a synchronous digital system have been considered. Nowadays, clock skew is among the main parameters that imposes restrictions in a digital system performance and reliability. It is actually one of the issues that requires more time of study.

At first, the role of a clock distribution network within a synchronous digital system was presented. A hierarchical clock distribution network, starting with the global part and finishing with the local clocking, was decided as the best option to implement a clock scheme since it allows the partition of the system in different functional sub-blocks. The advantages and disadvantages of the different strategies and topologies to implement a clock distribution network were discussed.

Secondly, an extensive analysis of the clock skew was performed. The theoretical background was described and their main sources were presented. One of the main goals of this work was to look for the existing models to estimate the clock skew in a clock distribution network. Three different models (statistical models according process and circuit variations) were studied and their equations were presented (models 1, 2 and 3).

The third part of this work was probably the most important. An extensive analysis of the models was realised thanks to different simulations in a generic H-tree (with optimized buffers and wires). They are usually utilized in the global part of a hierarchical clock distribution network. A java program, "*equations.java*", was specifically developed to calculate the clock skew estimations according to each model equations. Clock skew prediction for future technologies were made in a H-tree.

Concerning the models, model 1, which gives us an upper bound for the clock skew, and model 3, which gives an estimation that takes into account the correlation between clock paths, were compared in a H-tree with intermediate buffers. The main conclusion that could be drawn is that model 1 gave us a too conservative estimation compared to model 3. However, the validity of the simulations is dependent upon the accuracy of the

process and circuit variation parameters, which was probably the greatest difficulty found during the elaboration of the work. Model 2, which is applied to a tapered H-tree with widened wires, gave estimations smaller than the other two models. The reason is that a tapered H-tree has less clock skew sources (there are not buffers at the split points).

If models are applied to an H-tree for futures technologies, an important conclusion was drawn. Since clock skew increases rapidly for newer technologies due to the RC constant of buffers and wires increases considerably, a single H-tree is not appropriated for a low skew global clock distribution network. Additional techniques, like deskew circuits, are necessary to keep a low skew value within the system.

To finish, we can say that main goals of the work were achieved, but with the uncertainty of knowing if the clock skew value is realistic or not due to the difficulties of finding parameter values. The qualitative behaviour of the models has been described and checked.