

## Appendix 1

# Clock Skew Model 1

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## 1. Introduction

The accumulation of clock skew, the differences in arrival times of signal in digital systems with a central clock, is one of the factors that limit the speed in these systems.

These authors present a probabilistic model for the accumulation of clock skew in synchronous systems. Using this model, it's possible to estimate upper bounds for expected clock skew between processing elements in a processor array, and it's variance, in tree distribution systems with  $N$  synchronously clocked processing elements.

These results can be applied to two specific models for clock distributions:

- The first, *metric-free* model, the skew in a buffer stage is Gaussian with a variance independent of wire length. In this case, the upper bound on skew grows as  $\Theta(\ln^{3/2} N)$  for a system with  $N$  processing elements.
- The second, *metric* model, is intended to reflect VLSI constraints: the clock skew in a stage is Gaussian with a variance proportional to wire length. In this case the upper bound on expected skew is  $\Theta(\sqrt{N \ln N})$  for a system with  $N$  processors.

Thus the probabilistic model is more optimistic than the deterministic summation model of Fisher and Kung [FIS-85], which predict a clock skew  $\Theta(N)$  in this case, and is also consistent with their lower bound of  $\Omega(\sqrt{N})$  for planar embeddings. Fisher and Kung's model ignore a fundamental property of clock skew: its origins in the random variations of propagation time through buffers and wires.

## 2. General model of signal distribution

A global signal, such as clock, is distributed throughout a processing system by a signal distribution system. This, is composed of a number buffers (amplifiers) and wires which may be organized in a number of different ways. Two common structures are a bus and a tree.

A clock distribution system can be represented by a graph. It has a single distinguished vertex called the *source*. This is the origin of the global signal, and it's the only input to the distribution system. This distribution system can have multiple destinations, but for practical reasons, there is exactly one path from the source to each destination, that we are going to call *processing elements* (PE). PEs may have their own internal signal distribution system. This internal systems can be modelled in a similar manner to the global signal distribution system.

Each buffer and wire in the clock distribution system propagates and delays its incoming signal. Therefore, it's natural to associate every delay element in the signal distribution system, either a buffer or a wire, with a random variable,  $d_j$ . The value of the random variable gives the delay contribution of that element. The delay at any point is a real random variable, which is the sum of all the random variables along the path from the source to that point.

These definitions constitute the essence of the model. They make it very simple. But extremely general, and allow one to model any clock distribution system. Geometry can be incorporated into the model by attaching an appropriate probability density function to wire delays. There is also the freedom to analyze as much or as little as desired by

creating simplified models, in which buffer delays or wire delays can be ignored entirely.

The primary interest is the skew, the distribution of arrival times of a particular clock pulse to all PEs that communicate. Because the model is probabilistic, it's not possible to give an expression for the worst case skew, but we derive an expression for the expected maximum skew by assuming that all PEs communicate.

We haven't made any mention of any particular probability density function. The total delay through the distribution system is the sum of a number of random variables. In many cases, it quickly converges to a normal distribution, by the Central Limit Theorem. That's why, in the case of the skew computations, the actual distributions attached to buffers and wires are usually relatively unimportant.

The arrival times of a signal to the  $N$  PEs constitute a random sample of size  $N$ . From this sample, find the difference between the largest of them,  $A_{max}$ , and the smallest,  $A_{min}$ . The random variable  $R = A_{max} - A_{min}$  is called *range* of the sample. The range is equivalent to the skew in the signal distribution system.

### 3. Analysis and upper bounds

There is a lot of literature that describe techniques to compute the expected range of a set of independent identically distributed (iid) random variables. However, little is described about the case when variables are dependent, as they are in a clock tree. Fortunately, it is possible to use the statistics of iid variables to predict an upper bound on the statistics of the dependent variables. The relationship is given by the following theorem:

**Theorem 1:** *“The expected range of a set of random variables, which are dependent because they are sums of overlapping variables, is no greater than the expected range of the corresponding set of independent random variables”.*

We define  $y_i, i=1,2,\dots,N$  as iid real random variables, with  $N=kn$ , and  $\sigma_j, j=1,2,\dots,n$  as  $n$  disjoint subsets of different  $y_i$ , each of cardinality  $k$ . Now, we define  $\tau_i$  similarly, with  $k$  distinct elements each, except that they are not necessarily disjoint. Define the corresponding sums of the  $y_i$  by:

$$s_j = \sum_{y \in \sigma_j} y, \quad t_j = \sum_{y \in \tau_j} y$$

The **theorem 1** demonstrates that **the expected range of the  $s_j$  dominates the expected range of the  $t_j$** , and so any upper bound for the first also holds for the second. It's demonstrated using the following lemmas.

**Lemma 1:** *“If  $F_A(x)$  and  $F_B(x)$  are the probability distribution function for random variables  $A$  and  $B$ , and we suppose that  $F_A(x)$  and  $F_B(x)$  are differentiable and  $A$  and  $B$  have finite means and variances. Then, if  $F_A(x) \geq F_B(x)$  for all, then  $E(A) \leq E(B)$ ”.*

**Lemma 2:** *“For any  $\alpha$  and  $\beta$ , without any restriction in them, and any continuous probability density  $P$ :  $P(y \leq \alpha | y \leq \beta) \geq P(y \leq \alpha)$ . This lemma expresses that if  $y \leq \beta$ , then  $y \leq \alpha$ ”.*

Now that we have demonstrated this theorem, any bound for iid variables is an upper bound for the variables that arises in the clock distribution system model.

At this point we are going to assume that the arrival times are Gaussian, motivated by the Central Limit Theorem. Although no closed-form expression is known for the expected value and the variance of the range of  $N$  iid Gaussian distributed random variables, it is possible to obtain asymptotic expressions. This is shown by the following theorem.

**Theorem 2:** *“Let  $x_i, i=1,2,\dots,N$  be random samples from an  $n(\mu, \sigma^2)$  normal distribution, and let  $R = x_{max} - x_{min}$  be the difference of the largest and smallest  $x_i$ . Then the expected value of  $R$  is asymptotically:*

$$E[R] = \sigma \left[ \frac{4 \ln N - \ln \ln N - \ln 4\pi + 2C}{(2 \ln N)^{1/2}} + O\left(\frac{1}{\log N}\right) \right] \quad (1)$$

where  $C \approx 0.5772$  is Euler constant. The variance of  $R$  is given by:

$$\text{Var}[R] = \frac{\sigma^2}{\ln N} \frac{\pi^2}{6} + O\left[\frac{1}{\log^2 N}\right], \quad (2)$$

Equation (1) is therefore asymptotic upper bound on the expected skew in a clock distribution tree with  $N$  leaves.

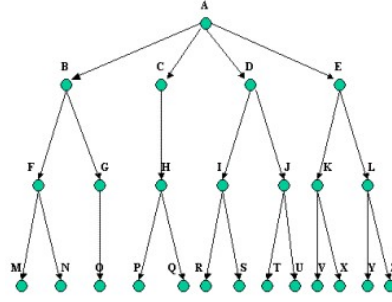
## 4. Examples

The model is applied to two different global signal distribution systems. The examples represent what it's considered to be common, typical clock distribution systems, but they are not intended to represent the full scope of all possibilities.

### 4.1. Metric-free tree

The first example is a metric-free tree. This type of topology could be used to implement a large-scale distribution system, which would provide a clock to chips on a board or to boards in a system. It doesn't constrain the circuit to be planar, so it's possible to equalize the lengths of all the wires in the tree. Therefore, every wire has the same probability distribution for delay, which can be lumped with the delay of the buffer that follows it. This results in a model of a tree of buffers without wires.

The root of the tree (node  $A$ ) is the source of the signal, the PEs are placed at the leaves (nodes  $M-Z$ ), and the intervening levels consist of buffers and wires. Figure 1 represents the tree:



**Figure 1: Clock distribution tree.**

In Figure 1, internal nodes are buffers, which retransmit the clock signal. The leaf nodes of the tree are the PEs that communicates among them. Lines connecting nodes of the clock tree represent wires that conduct the clock signal to all the PEs.

The delay through a buffer of the clock distribution tree can be modelled as a real random variable  $d_i$ , The arrival time of the clock signal to any PE is the sum of the delays along the path from the root of the tree to the PE. The buffers in this metric-free model cause all the delays. The effect of a wire is absorbed by the line effect of the buffer that follows it. The arrival time at leaf  $i$ ,  $A_i$ , is therefore the random variable:

$$A_i = \sum d_j, \text{ where the } d_j \text{ lie on the path from the root to the leaf } i.$$

In order to apply theorem 2, we must estimate the underlying distribution of the  $A_i$ .

Assuming that there are  $N$  PEs, each  $A_i$  is the sum of  $\log_2 N$   $d_j$ 's and that each  $d_j$  has mean  $\mu_b$  and variance  $\sigma_b^2$ . By our Gaussian assumption, the  $A_i$  have the distribution  $n(\mu_b \log_2 N, \sigma_b^2 \log_2^2 N)$ . Applying theorem 2 with distribution, we find that the expected skew is:

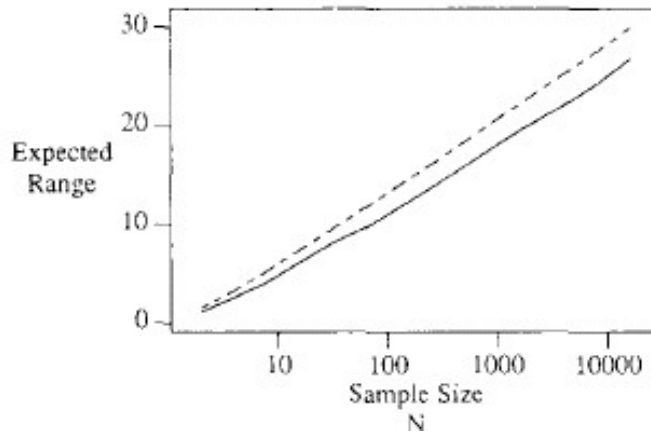
$$\begin{aligned} E[Skew] &= \sigma_b \log_2 N \left[ \frac{4 \ln N - \ln \ln N - \ln 4\pi + 2C}{(2 \ln N)^{1/2}} + O\left(\frac{1}{\log N}\right) \right] \\ &= \sigma_b \frac{4 \ln^{3/2} N}{\sqrt{2 \ln 2}} + \text{lower order terms} \\ &= \Theta(\ln^{3/2} N) \end{aligned} \tag{3}$$

The variance of the skew is:

$$\text{Var}[Skew] = \sigma_b^2 \frac{\pi^2}{6} + O\left[\frac{1}{\log^2 N}\right] \quad (4)$$

which is a constant when  $N \rightarrow \infty$ .

The following simulations corroborate the asymptotic skew results. Figure 2 shows the asymptotic curve of  $E[Skew]$ , with dashed line. The solid line represents the result of the Monte Carlo simulation after 100 trials. It shows that the bound is relatively tight, despite the fact that dependence between variables is ignored in the equation of  $E[Skew]$ . The gap between the asymptote and simulation results decreases steadily from about 20% for  $N=2^2$  to about 10% for  $N=2^{14}$ .



**Figure 2: Metric-free simulations.**

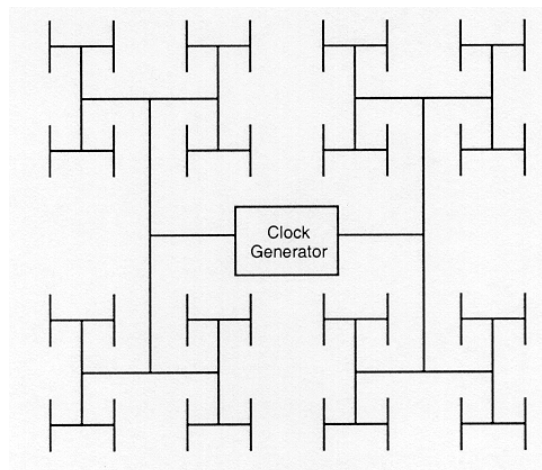
Even for trees of small depth, the expected range in both cases is nearly identical. This is due to the rapid convergence of the sums of random variables to a normal distribution.

The explicit inclusion of wire delays into the model (not to include wire delays with buffer delays) does not significantly modify the results. Wires can be considered to contribute an additional random delay at each level of the tree. Assuming that wire delays are distributed similarly to the buffer delays, the effect is to increase the variance

of the variance of the distribution of arrival times by a constant factor. This doesn't alter the asymptotic behaviour of skew.

## 4.2.Metric tree

The second example is a *metric* tree. This is the type of system that is typical of systems described for VLSI. The central assumption of this topology is that circuit must be embedded in the plane. If the embedding is to be area efficient, then the wires that connect buffers cannot be the same length everywhere. The delay through a wire therefore depends its location in he tree, and cannot be lumped with a buffer delay. A common tree of this type is the H-tree (Figure 3).



**Figure 3: H-tree clock distribution system.**

There are two distinct views of the effects of increasing system size (number of PEs) under the metric assumption. The first is to assume that a tree with an arbitrary number of leaves can be embedded in the fixed area of the integrated circuit. The alternative to this view sets a lower limit on the size of the smallest feature: in this case the size of a wire at the tree's leaves. Each preceding level is progressively larger (to avoid reflections in the wires) and the area of the entire clock tree grows with increasing system size. This view ignores the effects of shrinking feature size but its compatible with increases in this chip die size. We are going to adopt this second point of view.



Now we assume that buffer delay,  $d_j$ , is  $n(\mu_b, \sigma_b^2)$ . For this analysis we will also assume that wire delay,  $w_j$ , is Gaussian distributed with a mean value and a variance proportional to its length. The linear relationship for the variance can be justified by considering a long wire to be equivalent to two shorter wires placed end to end. The propagation delay of the long wire is equal to the sum of the propagation delays of the two shorter wires. The expected values add, as do the variances because the delays of the short wires are independent.

The wire delay at leaves of the tree is  $n(\mu_w, \sigma_w^2)$  distributed. Because wire length doubles at each higher level of the tree, the distribution of  $w_j$  can be written as function of the depth,  $d$ , of the wire. We find that  $w_j$ , is  $n\left(\mu_w \frac{N}{2^d}, \sigma_w^2 \left(\frac{N}{2^d}\right)^2\right)$ , where  $1 \leq d \leq \log_2 N$  and  $\mu_w$  and  $\sigma_w^2$  are the starting wire (lowest level) time delay mean and variance.

The total delay,  $A_i$ , is the sum of  $\log_2 N$  buffers delay and the sum delays from each level of the tree. In a H-tree, the root to leave distance, starting with a unit length at leaves, follows geometric series  $\left(1+1+2+2+4+4+\dots+\frac{\sqrt{N}}{2}+\frac{\sqrt{N}}{2}\right)=2(\sqrt{N}-1)$ . The total delay,  $A_i$ , therefore has the distribution:  $n\left(\mu_b \log_2 N + \mu_w 2(\sqrt{N}-1), \sigma_b^2 \log_2^2 N + \sigma_w^2 \left(2(\sqrt{N}-1)\right)^2\right)$ .

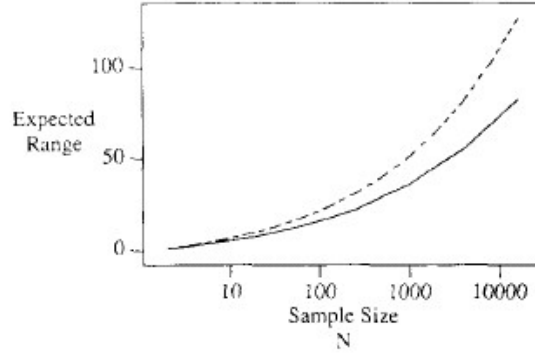
As  $N \rightarrow \infty$ , the linear (wire) term dominates. The expected skew is therefore:

$$\begin{aligned} E[Skew] &= \sigma_w 2(\sqrt{N}-1) \left[ \frac{4 \ln N - \ln \ln N - \ln 4\pi + 2C}{(2 \ln N)^{1/2}} + O\left(\frac{1}{\ln N}\right) \right] \\ &= \sigma_w \frac{8}{\sqrt{2}} (\sqrt{N}-1) \sqrt{\ln N} + \text{lower order terms} \\ &= \Theta(\sqrt{N \ln N}) \end{aligned} \quad (5)$$

and the variance is given by:

$$Var[Skew] = \frac{\sigma_w^2 2\sqrt{N}}{\ln N} \left( \frac{\pi^2}{6} \right) + O\left[ \frac{1}{\log N} \right] \quad (6)$$

Next Figure 4 shows the comparison of the H-tree asymptotic bound (dashed line) an Monte Carlo simulations (solid line) after 100 trials. In this case, the bound is not as tight as in the metric-free case, because the shared variables, representing deviation from the independence assumption, are near the root of the tree, where the wire lengths are longer.



**Figure 2: Metric simulations.**

### 4.3.Mistake probability

It's possible to give an estimate on the probability that the sample value of the skew is outside a certain range. Assume that  $X$  is a random variable with real mean  $\mu$  and variance  $\sigma^2$ . Then, using the one-sided Chebyshev inequality, we can predict un upper bound on the probability of exceeding the mean skew by an amount  $a$ :

$$P(X > (\mu + a)) \leq \frac{\sigma^2}{\sigma^2 + a^2} \quad (7)$$

Now let  $a=\alpha\mu$ , where  $\alpha$  is the fractional deviation from the expected value of skew. Then, using the estimate, in both the metric and metric-free case, we can have an estimate of an upper bound as  $N \rightarrow \infty$ :

$$P(X > (\mu + a)) \leq \frac{\frac{\pi^2}{6}}{\frac{\pi^2}{6} + 8\alpha^2 \ln^2 N} \quad (8)$$

## 5. Calculation

Now, we are going to show how to calculate the parameters necessary to apply the model.

### 5.1. Metric-free tree

In this model, I need the parameter  $\sigma_b^2$ , that is the delay variance through a buffer of the clock distribution tree (effect of the wire is absorbed by effect of the buffer).

Using Sakurai's model for interconnection delays, the delay of a stage composed of a wire interconnecting two buffers (inverters) is:

$$T_{\text{Delay}} = 1.02R_{\text{int}}C_{\text{int}} + 2.30(R_0C_0 + R_0C_{\text{int}} + R_{\text{int}}C_0) \quad (9)$$

where  $R_{\text{int}}$  and  $C_{\text{int}}$  are the total resistance and capacitance of the interconnecting wire,  $R_0$  is the on-resistance of the driving transistor, and  $C_0$  is the input capacitance of the driving inverter.

$$R_0 \approx \frac{L_{\text{eff}}/W}{\mu C_{\text{ox}}(V_{\text{DD}} - V_T)}, \quad C_0 = C_{\text{ox}} \cdot W \cdot L_{\text{eff}}, \quad R_{\text{int}} = \frac{\rho}{W_{\text{int}} t_{\text{int}}} L_{\text{int}}, \quad C_{\text{int}} = \frac{\epsilon_r W_{\text{int}}}{T_{\text{ILD}}} L_{\text{int}} \quad (10)$$

Here,  $L_{\text{int}}$  is the length of the wire at the last stage of the H-tree.

We are going to consider the following variables to calculate  $T_{\text{delay}}$ :

- $V_T$ : threshold voltage.
- $t_{\text{ox}}$ : gate oxide thickness.
- $L_{\text{eff}}$ : transistors effective length.
- $V_{\text{DD}}$ : power supply voltage.
- $T_{\text{ILD}}$ : interlevel dielectric thickness.
- $W_{\text{int}}$ : wire width variation.
- $t_{\text{int}}$ : wire thickness variation.

We also consider them independent. Therefore, variance of  $T_{delay}$  ( $\sigma_b^2$ ) can be determined in terms of variances of these independent random variables.

$$\begin{aligned} \sigma_b^2 = \sigma_{T_{Delay}}^2 = & \left( \frac{\partial T_{Delay}}{\partial V_T} \right)^2 \sigma_{V_T}^2 + \left( \frac{\partial T_{Delay}}{\partial t_{ox}} \right)^2 \sigma_{t_{ox}}^2 + \left( \frac{\partial T_{Delay}}{\partial L_{eff}} \right)^2 \sigma_{L_{eff}}^2 \\ & + \left( \frac{\partial T_{Delay}}{\partial V_{DD}} \right)^2 \sigma_{V_{DD}}^2 + \left( \frac{\partial T_{Delay}}{\partial T_{ILD}} \right)^2 \sigma_{T_{ILD}}^2 + \left( \frac{\partial T_{Delay}}{\partial W_{int}} \right)^2 \sigma_{W_{int}}^2 + \left( \frac{\partial T_{Delay}}{\partial t_{int}} \right)^2 \sigma_{t_{int}}^2 \end{aligned} \quad (11)$$

where:

$$\begin{aligned} \frac{\partial T_{Delay}}{\partial V_T} &= \frac{\partial T_{Delay}}{\partial R_0} \frac{\partial R_0}{\partial V_T} = 2.30(C_0 + C_{int}) \frac{R_0}{V_{DD} - V_T} \\ \frac{\partial T_{Delay}}{\partial t_{ox}} &= \frac{\partial T_{Delay}}{\partial R_0} \frac{\partial R_0}{\partial t_{ox}} + \frac{\partial T_{Delay}}{\partial C_0} \frac{\partial C_0}{\partial t_{ox}} = 2.30(C_0 + C_{int}) \frac{R_0}{t_{ox}} + 2.30(R_0 + R_{int}) \frac{C_0}{t_{ox}} \\ \frac{\partial T_{Delay}}{\partial L_{eff}} &= \frac{\partial T_{Delay}}{\partial R_0} \frac{\partial R_0}{\partial L_{eff}} + \frac{\partial T_{Delay}}{\partial C_0} \frac{\partial C_0}{\partial L_{eff}} = 2.30(C_0 + C_{int}) \frac{R_0}{L_{eff}} + 2.30(R_0 + R_{int}) \frac{C_0}{L_{eff}} \\ \frac{\partial T_{Delay}}{\partial V_{DD}} &= \frac{\partial T_{Delay}}{\partial R_0} \frac{\partial R_0}{\partial V_{DD}} = 2.30(C_0 + C_{int}) \frac{R_0}{V_{DD} - V_T} \\ \frac{\partial T_{Delay}}{\partial T_{ILD}} &= \frac{\partial T_{Delay}}{\partial C_{int}} \frac{\partial C_{int}}{\partial T_{ILD}} = (1.02R_{int} + 2.30R_0) \frac{C_{int}}{T_{ILD}} \\ \frac{\partial T_{Delay}}{\partial W_{int}} &= \frac{\partial T_{Delay}}{\partial R_{int}} \frac{\partial R_{int}}{\partial W_{int}} + \frac{\partial T_{Delay}}{\partial C_{int}} \frac{\partial C_{int}}{\partial W_{int}} = (1.02C_{int} + 2.30C_0) \frac{R_{int}}{W_{int}} + (1.02R_{int} + 2.30R_0) \frac{C_{int}}{W_{int}} \\ \frac{\partial T_{Delay}}{\partial t_{int}} &= \frac{\partial T_{Delay}}{\partial R_{int}} \frac{\partial R_{int}}{\partial t_{int}} = (1.02C_{int} + 2.30C_0) \frac{R_{int}}{t_{int}} \end{aligned} \quad (12)$$

## 5.2.Metric tree

In the second model, we need the parameter  $\sigma_w^2$  that is the delay variance through a wire of the clock distribution tree. Buffer delay is not necessary to be taken into account because, in this model, the wire effect dominates.

Using Sakurai's model for interconnection delays, the delay of a stage composed of a wire interconnecting two buffers (inverters) is:

$$T_{\text{Delay}} = 1.02R_{\text{int}}C_{\text{int}} + 2.30(R_0C_0 + R_0C_{\text{int}} + R_{\text{int}}C_0) \quad (13)$$

where  $R_{\text{int}}$  and  $C_{\text{int}}$  are the total resistance and capacitance of the interconnecting wire,  $R_0$  is the on-resistance of the driving transistor, and  $C_0$  is the input capacitance of the driven inverter.

$$R_0 \approx \frac{L_{\text{eff}} / W}{\mu C_{\text{ox}} (V_{\text{DD}} - V_T)}, \quad C_0 = C_{\text{ox}} \cdot W \cdot L_{\text{eff}}, \quad R_{\text{int}} = \frac{\rho}{W_{\text{int}} t_{\text{int}}} L_{\text{int}}, \quad C_{\text{int}} = \frac{\epsilon_r W_{\text{int}}}{T_{\text{ILD}}} L_{\text{int}} \quad (14)$$

Here,  $L_{\text{int}}$  is the length of the wire at the last stage of the H-tree.

We are going to consider the following variables (Only the variables that affect to  $R_{\text{int}}$  and  $C_{\text{int}}$ , because we only consider the wire's delay) to calculate  $T_{\text{delay}}$ :

- $T_{\text{ILD}}$ : interlevel dielectric thickness.
- $W_{\text{int}}$ : wire width variation.
- $t_{\text{int}}$ : wire thickness variation.

We also consider them independent. Therefore, variance of  $T_{\text{delay}}$  can be determined in terms of variances of these independent random variables.

$$\sigma_w^2 = \sigma_{T_{\text{Delay}}}^2 = \left( \frac{\partial T_{\text{Delay}}}{\partial T_{\text{ILD}}} \right)^2 \sigma_{T_{\text{ILD}}}^2 + \left( \frac{\partial T_{\text{Delay}}}{\partial W_{\text{int}}} \right)^2 \sigma_{W_{\text{int}}}^2 + \left( \frac{\partial T_{\text{Delay}}}{\partial t_{\text{int}}} \right)^2 \sigma_{t_{\text{int}}}^2 \quad (15)$$

where:

$$\begin{aligned} \frac{\partial T_{\text{Delay}}}{\partial T_{\text{ILD}}} &= \frac{\partial T_{\text{Delay}}}{\partial C_{\text{int}}} \frac{\partial C_{\text{int}}}{\partial T_{\text{ILD}}} = (1.02R_{\text{int}} + 2.30R_0) \frac{C_{\text{int}}}{T_{\text{ILD}}} \\ \frac{\partial T_{\text{Delay}}}{\partial W_{\text{int}}} &= \frac{\partial T_{\text{Delay}}}{\partial R_{\text{int}}} \frac{\partial R_{\text{int}}}{\partial W_{\text{int}}} + \frac{\partial T_{\text{Delay}}}{\partial C_{\text{int}}} \frac{\partial C_{\text{int}}}{\partial W_{\text{int}}} = (1.02C_{\text{int}} + 2.30C_0) \frac{R_{\text{int}}}{W_{\text{int}}} + (1.02R_{\text{int}} + 2.30R_0) \frac{C_{\text{int}}}{W_{\text{int}}} \\ \frac{\partial T_{\text{Delay}}}{\partial t_{\text{int}}} &= \frac{\partial T_{\text{Delay}}}{\partial R_{\text{int}}} \frac{\partial R_{\text{int}}}{\partial t_{\text{int}}} = (1.02C_{\text{int}} + 2.30C_0) \frac{R_{\text{int}}}{t_{\text{int}}} \end{aligned} \quad (16)$$

## 6. Conclusions

- The model is probabilistic.
- It give us an estimation of upper bounds for expected clock skew in tree distribution systems with  $N$  synchronously clocked processing elements.
- Three basic assumptions in our model:
  - The paths from the clock source to the processing elements are identical, in the sense that the paths are equal of length, contain the same number of wires and buffer stages, and equally loaded.
  - The clock arrival times are random variables, and are the sums of uncertain independent delays through many wires and buffers. By the Central Limit Theorem, the arrival time of clock signals at processors can be modelled asymptotically as a Gaussian random variable.
  - For the purpose of arriving at an upper bound on clock skew that is independent of topology, we make the additional assumption that any processor can communicate with any other.
- Results are applied to two different cases:
  - Metric-free model: Total delay in each buffer stage is Gaussian with a variance independent of stage number. Upper bound grows as  $\Theta(\log N)$ .
  - Metric model: Clock delay in a stage is Gaussian with a variance proportional to wire length. H-tree case. Upper bound grows  $\Theta(\sqrt{\sqrt{N} \log N})$ .
- To apply the model it's necessary to know:

- Metric-free model
  - $N$ : Number of processing elements.
  - $\sigma_b^2$ : Delay variance through a buffer of the clock distribution tree (effect of the wire is absorbed by effect of the buffer).
- Metric model
  - $N$ : Number of processing elements.
  - $\sigma_w^2$ : Delay variance through a wire (effect of the buffers is not taken into account).
- We can calculate an upper bound of the clock skew for a H-tree clock distribution network taking into account the buffer delay. It is very recommendable, because the model doesn't consider a real case, where to increase the number of levels doesn't imply that the die size increases. To increase the number of levels supposes that all the branches are shorter, so their delay is reduced. It makes no sense the metric-free supposition that when  $N \rightarrow \infty$ , the wire term dominates.

In this case, including buffer delays, the upper bound clock skew expression would be:

$$E[Skew] = \left( \sigma_b \log_2 N + \sigma_w 2(\sqrt{N} - 1) \right) \left[ \frac{4 \ln N - \ln \ln N - \ln 4\pi + 2C}{(2 \ln N)^{1/2}} + O\left(\frac{1}{\ln N}\right) \right] \quad (17)$$

Now, to calculate  $\sigma_w^2$ , we have to calculate the variance of  $T_{Delay}$  as function of buffer parameter variations ( $V_T$ ,  $t_{ox}$ ,  $L_{eff}$ , and  $V_{DD}$ ). To compute this variations, we do in the same way that in the metric-free model (equations 12).

- Parameters we need to know:
  - Interconnection resistance:  $R_{int}$
  - Interconnection capacitance:  $C_{int}$
  - On-resistance of the driving transistor:  $R_0$

- Input capacitance of the driving inverter:  $C_0$
- Threshold voltage of inverters:  $V_T$
- Power supply voltage:  $V_{DD}$
  
- Threshold voltage deviation (in %):  $\sigma_{VT}$
- Power supply voltage deviation (in %):  $\sigma_{VDD}$
- Gate oxide thickness deviation (in %):  $\sigma_{tox}$
- Effective channel length deviation (in %):  $\sigma_{Leff}$
- ILD thickness deviation (in %):  $\sigma_{TILD}$
- Wire width deviation (in %):  $\sigma_{wint}$
- Wire thickness deviation (in %):  $\sigma_{tint}$
  
- Number of processing elements:  $N$
- Lowest level branch length:  $L_{int}$