Proyecto Fin de Carrera:

Anexo 2: Datasheets.

Mesa de Mezclas Digital Vía USB .

Alumno: Sebastián Ramiro Utrera.

Departamento de Ingeniería Electrónica.

FAIRCHILD
SEMICONDUCTOR®

LM317
3-Terminal Positive Adjustable Regulator

March 2000

Revised June 2005

General Description

This monolithic integrated circuit is an adjustable 3-terminal positive voltage regulator designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V. It employs internal current limiting, thermal shut-down and safe area compensation.

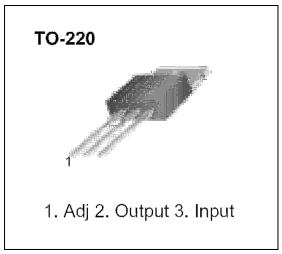
Features

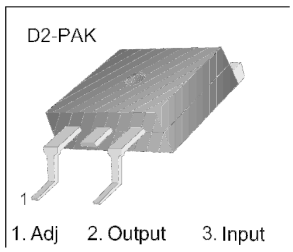
- Output Current In Excess of 1.5A
- Output Adjustable Between 1.2V and 37V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe Operating Area Compensation
- TO-220 Package
- D2 PAK Package

Ordering Code:

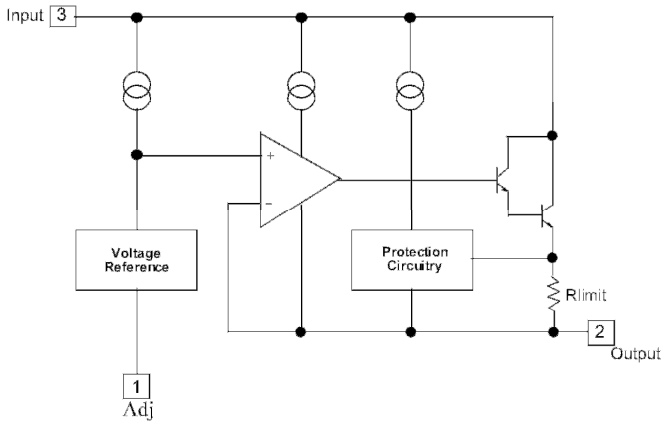
Product Number	Package	Operating Temperature
LM317T	TO-220	0qC to 125qC
LM317D2TXM	D2 PAK	0qC to 125qC

Connection Diagrams





Internal Block Diagram



© 2005 Fairchild Semiconductor Corporation

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input-Output Voltage Differential	$V_I - V_O$	40	V
Lead Temperature	T_{LEAD}	230	qC
Power Dissipation	P_D	Internally limited	W
Operating Junction Temperature Range	T_j	0 a 125	qC
Storage Temperature Range	T_{STG}	65 a 125	qC
Temperature Coefficient of Output Voltage	$\bullet V_O/\bullet T$	r0.02	% / qC

Note 1: Absolute Maximum Ratings: are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Electrical Characteristic

($V_I - V_O$ 5V, I_O 0.5A, 0qC d T_J d 125qC, I_{MAX} 1.5A, P_{DMAX} 20W, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Line Regulation (Note 2)	Rline	T_A 25qC 3V d V_I V_O d 40V	—	0.01	0.04	% / V
		3V d V_I V_O d 40V	–	0.02	0.07	% / V
Load Regulation (Note 2)	Rload	T_A 25qc, 10mA d I_O d I_{MAX} V_O 5V V_O t 5V	–	18.0 0.4	25.0 0.5	mV% / V_O
		10mA d I_O d I_{MAX} V_O 5V V_O t 5V	–	40.0 0.8	70.0 1.5	mV% / V_O
Adjustable Pin Current	I_{ADJ}	–	–	46.0	100	PA
Adjustable Pin Current Change	$\bullet I_{ADJ}$	3V d V_I V_O d 40V 10mA d I_O d I_{MAX} P_D d P_{MAX}	–	2.0	5.0	PA
Reference Voltage	V_{REF}	3V d V_{IN} - V_O d 40V 10mA d I_O d I_{MAX} P_D d P_{MAX}	1.20	1.25	1.30	V
Temperature Stability	ST_T	–	–	0.7	–	% / V_O
Minimum Load Current to Maintain Regulation	$I_{L(MIN)}$	$V_I - V_O$ 40V	–	3.5	12.0	mA
Maximum Output Current	$I_{O(MAX)}$	$V_I - V_O$ d 15V, P_D d P_{MAX} $V_I - V_O$ d 40V, P_D d P_{MAX} T_A 25qC	1.0	2.2 0.3	–	A
RMS Noise,% of V_{OUT}	eN	T_A 25qC, 10Hz d f d 10KHz	–	0.003	0.01	% / V_O
Ripple Rejection	RR	V_O 10V, f 120Hz without C_{ADJ} C_{ADJ} 10PF (Note 3)	66.0	60.0 75.0	–	dB
Long-Term Stability, T_J T_{HIGH}	ST	T_A 25qC for end point measurements, 1000HR	–	0.3	1.0	%
Thermal Resistance Junction to Case	R_{TJC}	–	–	5.0	–	qC / W

Note 2: Load and line regulation are specified at constant junction temperature. Change in V_D due to heating effects must be taken into account separately. Pulse testing with low duty is used. (P_{MAX} 20S)

Note 3: CADJ, when used, is connected between the adjustment pin and ground.

Typical Performance Characteristics

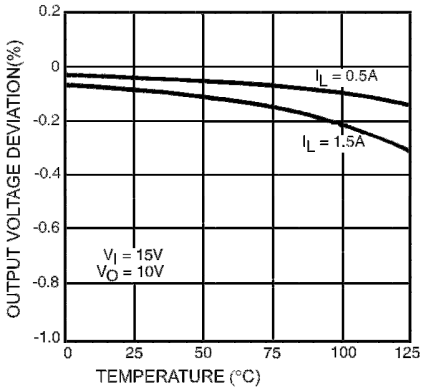


FIGURE 1. Load Regulation

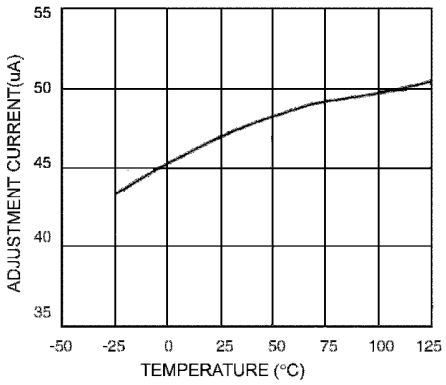


FIGURE 2. Adjustment Current

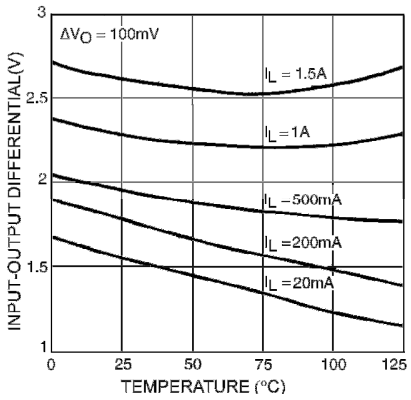


FIGURE 3. Dropout Voltage

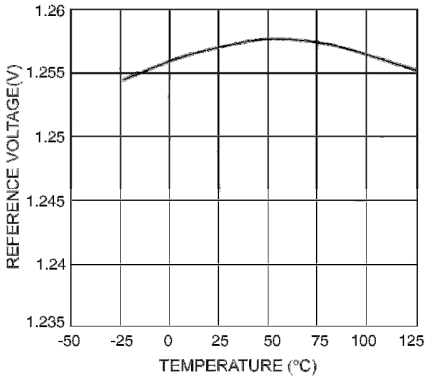
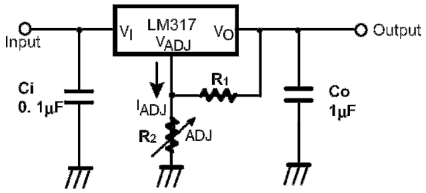


FIGURE 4. Reference Voltage

Typical Application



$$V_O = 1.25V\ (1 + R_2 / R_1) + I_{ADJ}\ R_2$$

Note: C_i is required when regulator is located an appreciable distance from power supply filter.

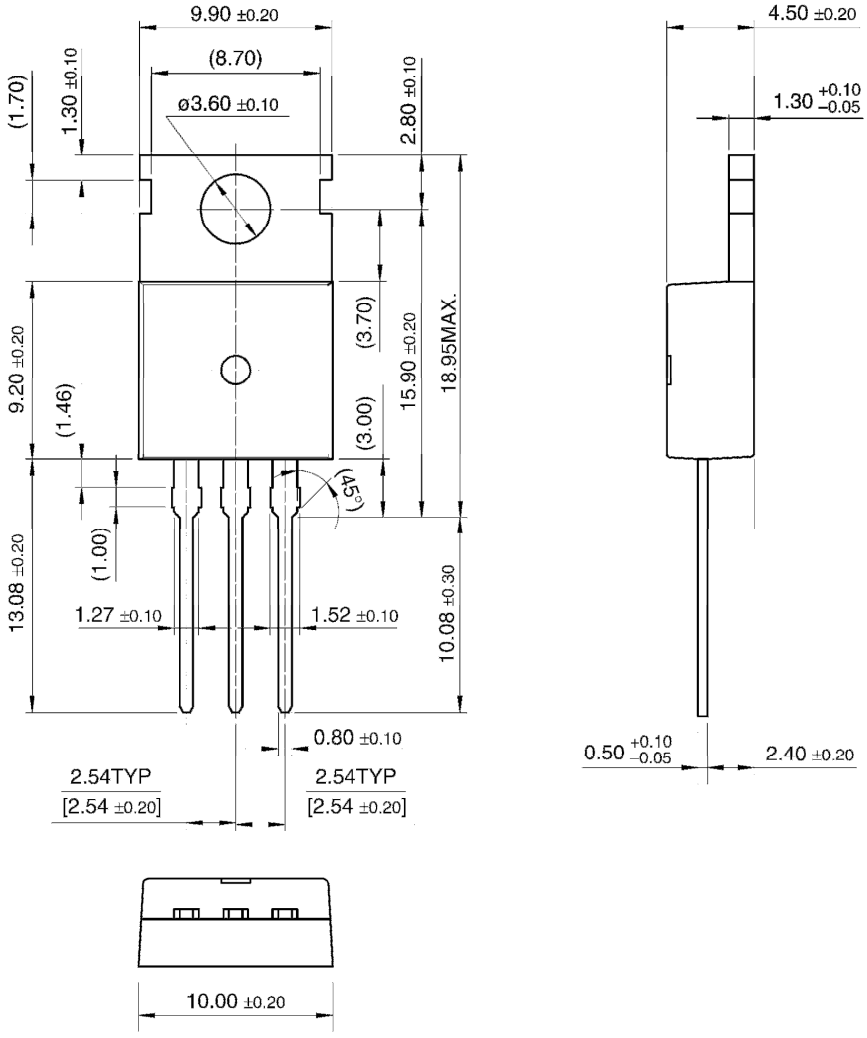
Note: C_o is not needed for stability, however, it does improve transient response.

Note: Since I_{ADJ} is controlled to less than 100PA, the error associated with this term is negligible in most applications.

FIGURE 5. Programmable Regulator

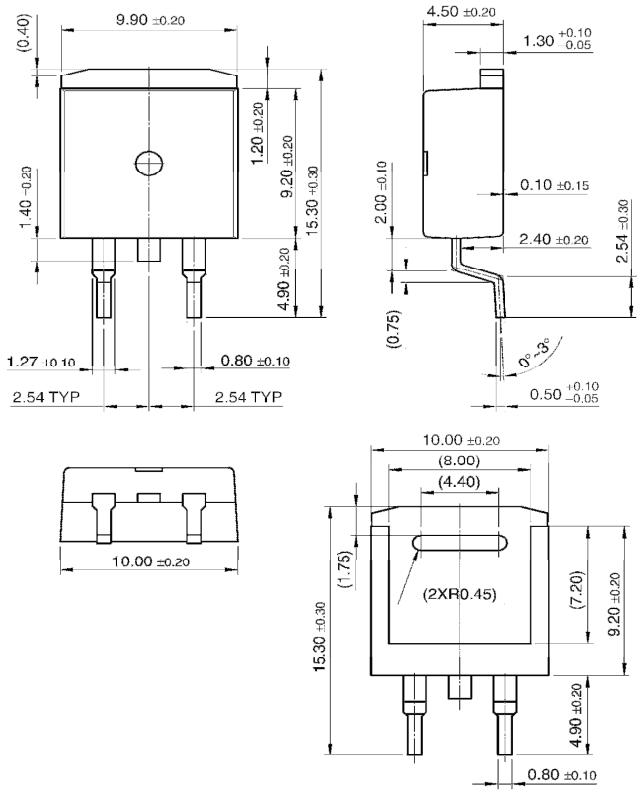
Physical Dimensions inches (millimeters) unless otherwise noted

TO-220



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

D^2-PAK



Dimensions in Millimeters

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

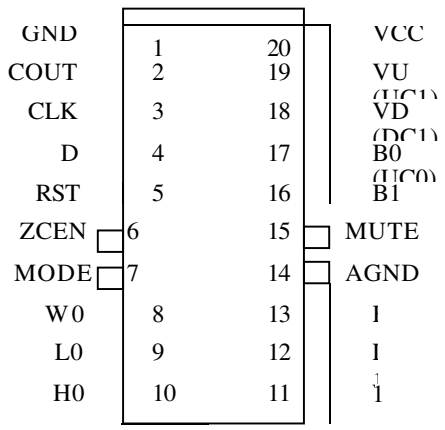
www.fairchildsemi.com

DS1802
Dual Audio Taper Potentiometer With Pushbutton Control

FEATURES

- Ultra-low power consumption
- Operates from 3V or 5V supplies
- Two digitally controlled, 65-position potentiometers including mute
- Logarithmic resistive characteristics (1 dB per step)
- Zero-crossing detection eliminates noise caused by wiper movement
- Digital or mechanical pushbutton wiper control
- Serial port provides means for setting and reading both potentiometers wipers
- 20-pin SOIC and 20-pin TSSOP for surface mount applications
- Operating Temperature Range: -40°C to +85°C
- Software and hardware mute
- Resistance Available: 45 kΩ

PIN ASSIGNMENT



20-Pin DIP (300-mil)
20-Pin SOIC (300-mil)
20-Pin TSSOP (173-mil)
See Mech. Drawings Section

PIN DESCRIPTION

L0, L1	-	Low End of Resistor
H0, H1	-	High End of Resistor
W1,W2	-	Wiper End of Resistor
V_{CC}	-	3V/5V Power Supply Input
$\overline{RST}$	-	Serial Port Reset Input
D	-	Serial Port Data Input
CLK	-	Serial Port Clock Input
MODE	-	Mode Select Input
UC0, UC1	-	Up Control Pushbutton Inputs
DC0, DC1	-	Down Control Pushbutton Inputs
VU, VD	-	Volume-Up/Volume-Down Inputs
B0, B1	-	Balance Pot-0, Pot-1 Inputs
GND	-	Digital Ground
MUTE	-	Mute
AGND	-	Analog Ground
$\overline{ZCEN}$	-	Zero-Crossing Detect Input
C_{OUT}	-	Cascade Output

DESCRIPTION

The DS1802 is a dual audio taper-potentiometer having logarithmic resistive characteristics over the device range. Each potentiometer provides 65 wiper positions with a 1 dB increment per step and device mute. The DS1802 has two methods of device control, which include contact closure (pushbutton) inputs and a 3-wire serial interface for wiper positioning. The pushbutton control inputs provide a simple interface for device control without the need for a CPU. While the 3-wire serial interface, using a CPU, provides the user the ability of reading or writing exact wiper positions of the two potentiometers. The DS1802 can also be configured to operate in either independent or "stereo" modes when using pushbutton control. Independent mode of operation allows for independent wiper control, and stereo mode of operation provides single input control over both potentiometer wiper positions. The DS1802 is offered in commercial temperature versions. Packages for the part include a 20-pin DIP, 20-pin SOIC, and 20-pin TSSOP.

OPERATION

The DS1802 provides two 65-position potentiometers per package, each having a logarithmic resistive characteristic as shown in Table 1. The DS1802 can be controlled either digitally or mechanically using a 3-wire serial interface or contact closure input, respectively. The pushbutton interface allows for a simple mechanical control method for incrementing or decrementing wiper position. The 3-wire serial interface is designed for CPU controlled applications and allows the potentiometer's exact wiper position to be read or written. Additionally, the DS1802 can be daisy-chained for multi-device environments.

Figure 1 presents a block diagram of the DS1802. As shown, the inputs from the 3-wire serial interface and contact closure inputs drive a command/control unit. The command/control unit interprets these inputs for control of the two potentiometers.

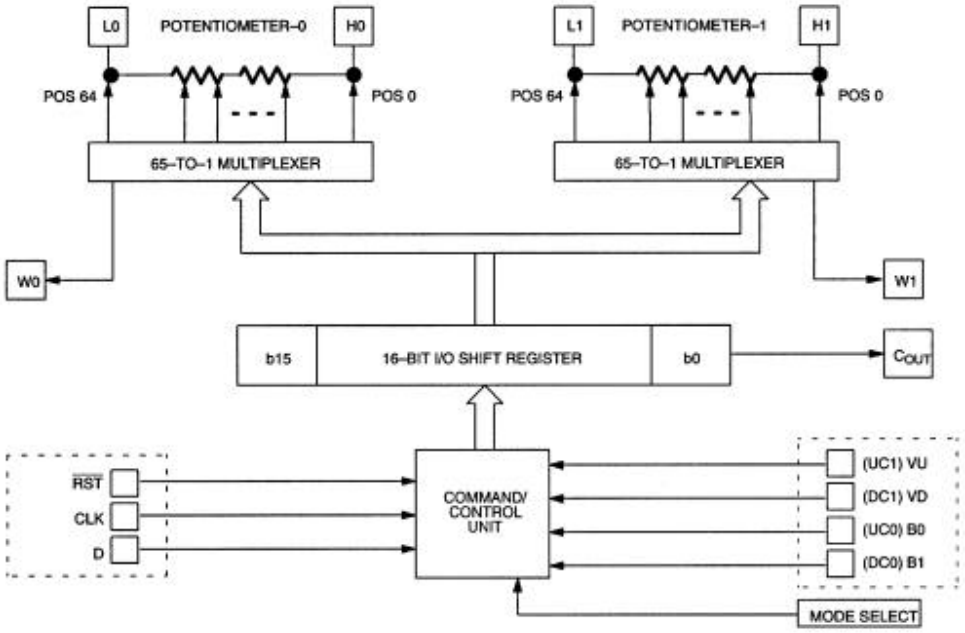
The MODE input is used for contact closure operation. This input allows the user to choose between independent mode control and stereo mode control. The MODE input is discussed in detail under the contact closure interface control.

On power-up the serial port is stable and active within 10 microseconds. The contact closure control interface inputs are active after 50 ms. The wiper position on power-up will be at position 63, the low end of the potentiometer. Position 64 is the mute level.

RESISTANCE CHARACTERISTICS Table 1

POSITION	OUTPUT LEVEL (dB)
0	0
1	-1
2	-2
3	-3
4	-4
5	-5
•	•
•	•
•	•
63	-63
64(mute)	<-90

DS1802 BLOCK DIAGRAM Figure 1



CONTACT CLOSURE INTERFACE CONTROL

The DS1802 can be configured to operate from contact closure inputs sometimes referred to as pushbutton control. There exists a total of four physical contact closure terminals on the device package. When combined with the MODE input, these contact closure inputs provide a total of eight different contact closure functions. These eight contact closure functions are listed in Table 2.

CONTACT CLOSURE INPUTS Table 2

CONTACT INPUT	DESCRIPTION
UC0*	Up contact potentiometer-0
UC1*	Up contact potentiometer-1
DC0*	Down contact potentiometer-0
DC1*	Down contact potentiometer-1
VU**	Volume-up
VD**	Volume-down
B0**	Balance Pot-0
B1**	Balance Pot-1

* independent mode control

** stereo mode control

The MODE input terminal is used to select the mode of wiper control using contact closure. There exist two modes of wiper control, which include independent mode control and stereo mode control. As shown in the pin assignment diagram, the contact closure inputs share pins. Input functionality is determined by the state of the MODE input at power-up.

Independent mode control allows the user to independently control each potentiometer's wiper position. For independent mode control, the MODE input should be in a high state. For stereo mode control, the MODE input should be in a low state. The input should always be tied to a well-defined logic state.

The contact closure inputs which affect independent mode control include UC0, UC1, DC0, and DC1. As outlined in Table 2, the UC0 and UC1 inputs are used to move the potentiometers wipers towards the high end of the potentiometer (H0, H1) terminals. The DC0 and DC1 inputs control movement towards the low-end terminals (L0, L1). Note that UC0 and DC0 control potentiometer-0 wiper movement while UC1 and DC1 control potentiometer-1 movement.

An additional feature of the contact closure interface is the ability to control both directions of wiper movement with only the UC0 and UC1 contact closure inputs. This feature is referred to as single pushbutton operation. Figure 2(a) and (b) illustrates both configurations for single pushbutton and dual pushbutton operation.

Stereo Mode Control

Stereo mode control allows for the simultaneous positioning of both potentiometer wipers from a single control input. Stereo mode control is entered when the MODE select input is in a low state at power-up. The functionality available when operating in stereo mode control includes: 1) volume-up, 2) volume- down, 3) balance-0, and 4) balance-1.

Volume Control Inputs

Volume-up and volume-down allow the user to move both wipers either up or down the resistor array without changing the relative balance or distance between the wipers. For example, if potentiometer-0's wiper is set at position 28 and potentiometer-1's wiper is set at position 20, the position distance of eight is maintained when using either of these functions. Additionally, the balance between both wipers is preserved if either reaches the end of its resistor array.

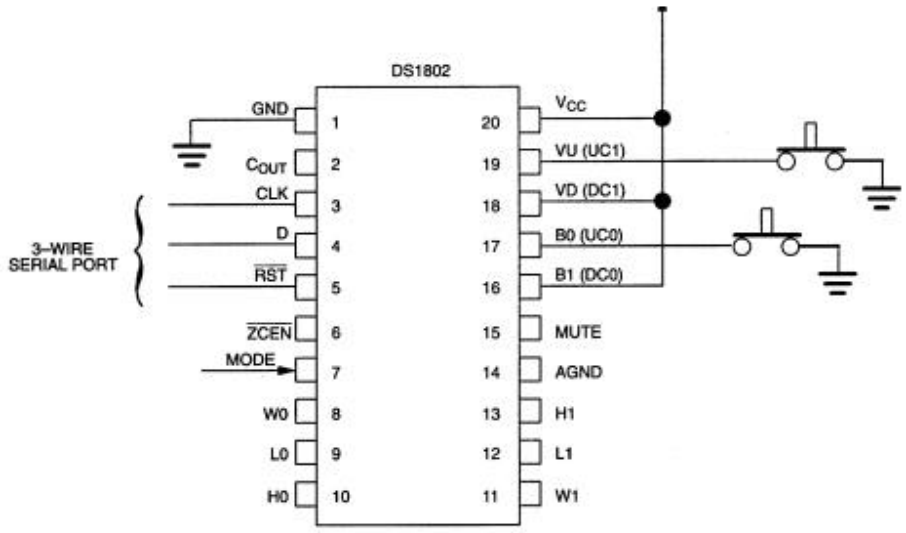
Balance Control Inputs

Balance control inputs allow the user to control the distance or offset between potentiometer-0 and potentiometer-1 wiper position settings. The two input controls for balance include B0 and B1. The balance control inputs attempt to minimize their respective wiper's attenuation. When the DS1802 first receives a balance control input, the position of the wiper closest to the high end terminal, H X , is stored. Wiper position movement is then governed by this stored value.

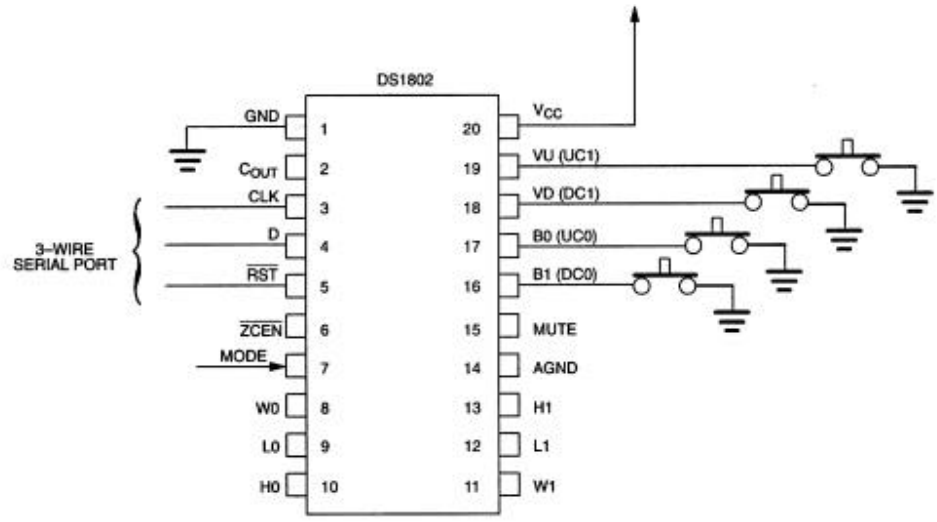
For example, if the B0 input is used, the attenuation of potentiometer-0 will change only if it is greater than the attenuation of potentiometer-1. The direction of movement for the potentiometer-0 wiper will be towards the high end of the resistor array. Movement of wiper-0 will only stop once its value is equal to that of wiper-1. At this point, continued input activity on the B0 input will cause an increase in attenuation of potentiometer-1. Note that if the wiper of potentiometer-1 peaks at the bottom of its array, continued B0 input activity will cause no change in the wiper positions of the device. A B1 input will be required to change the balance of the two wipers if the potentiometer wiper peaks in this case.

In the case where both wiper positions are at position 63, no movement of the wipers will take place when using the balance controlled inputs. A volume- up control input is required to move the wiper positions from the bottom of the resistor arrays. Balance control operation is presented in Figure 3.

SINGLE PUSHBUTTON CONFIGURATION Figure 2(a)



DUAL PUSHBUTTON CONFIGURATION Figure 2(b)



Contact closure is defined as the transition from a high level to a low level on the contact closure input terminals. The DS1802 interprets input pulse widths as the means of controlling wiper movement. A single pulse input over the UCx or DCx input terminals will cause the wiper to move one position. A transition from high to low on these inputs is considered the beginning of pulse activity or contact closure. A single pulse is defined as being greater than 1 ms but lasting no longer than a second. This is shown is Figure 4(a).

Repetitive pulsed inputs can be used to step through each resistive position of the device in a relatively fast manner (see Figure 4(b)). The requirement for repetitive pulsed inputs is that pulses must be separated by a minimum time of 1 ms. If not, the DS1802 will interpret repetitive pulses as a single pulse.

Pulse inputs lasting longer than 1 second will cause the wiper to move one position every 100 ms following the initial 1 second hold time. The total time to transcend the entire potentiometer using a continuous input pulse is given by the formula below:

1 (second) + 63 X 100 ms =7.3 (seconds)

Single Contact Closure

Single contact closure operation allows the user to control wiper movement in either direction from a single pushbutton input. Figure 2(a), as mentioned, presents a typical single pushbutton configuration.

In independent mode control, the UC0 and UC1 inputs are used to increment and decrement each respective wiper position for single pushbutton mode of operation. The DC0 and DC1 inputs provide no functionality in the single pushbutton configuration but must be connected to the positive supply voltage (V_{CC}). In stereo mode control, the VU and B0 inputs are used to control volume and balance. The VD and B1 inputs provide no functionality in the single pushbutton configuration but must be connected to the positive supply voltage (V_{CC}). The 3-wire serial port inputs ($\overline{RST}$, CLK, and D) must be grounded when not used.

On device power-up, the configuration shown in Figure 2(a) must exist in order to enter the single contact closure mode of operation; especially and specifically, the (DC0, DC1, VD, and B1) input's connection to the positive supply voltage (V_{CC}).

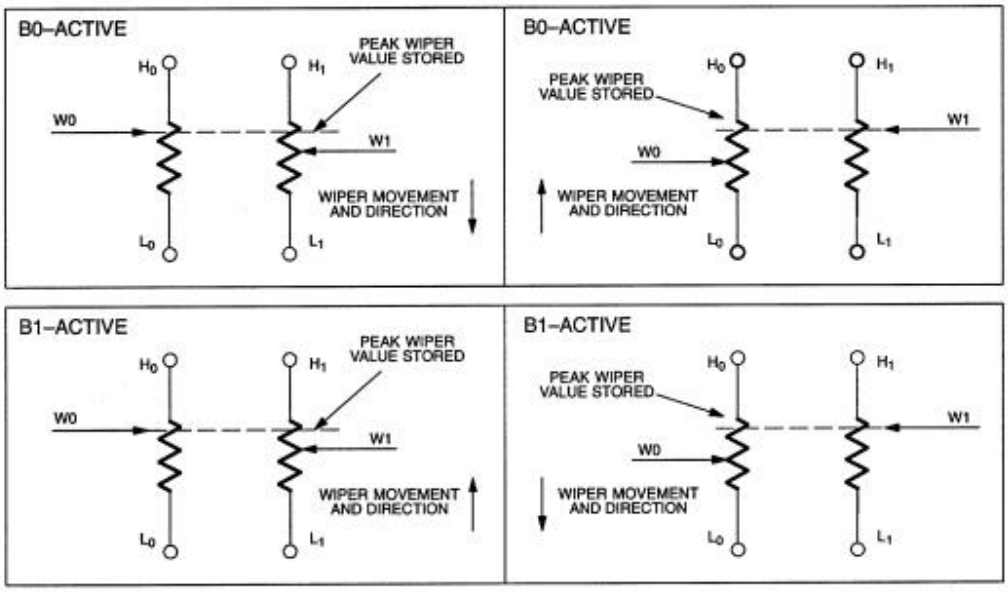
The direction of wiper movement in single pushbutton operation is determined by prior activity; with the direction of wiper movement being opposite to that of the previous activity.

Changing the direction of wiper movement in single pushbutton configuration is accomplish by a period of inactivity on the controlling input of a (minimum) 1 second or greater. For example, when operating from independent mode control, an inactivity of 1 second or greater on the UC0 input will cause the direction of the potentiometer-0 wiper to reverse. The same is true for the UC1 input. Also, in independent mode control and single pushbutton configuration, as the wiper reaches the end of the potentiometer range its direction of movement reverses. This will occur regardless of whether the input is a continuous pulse, a sequence of repetitive pulses or a single pulse.

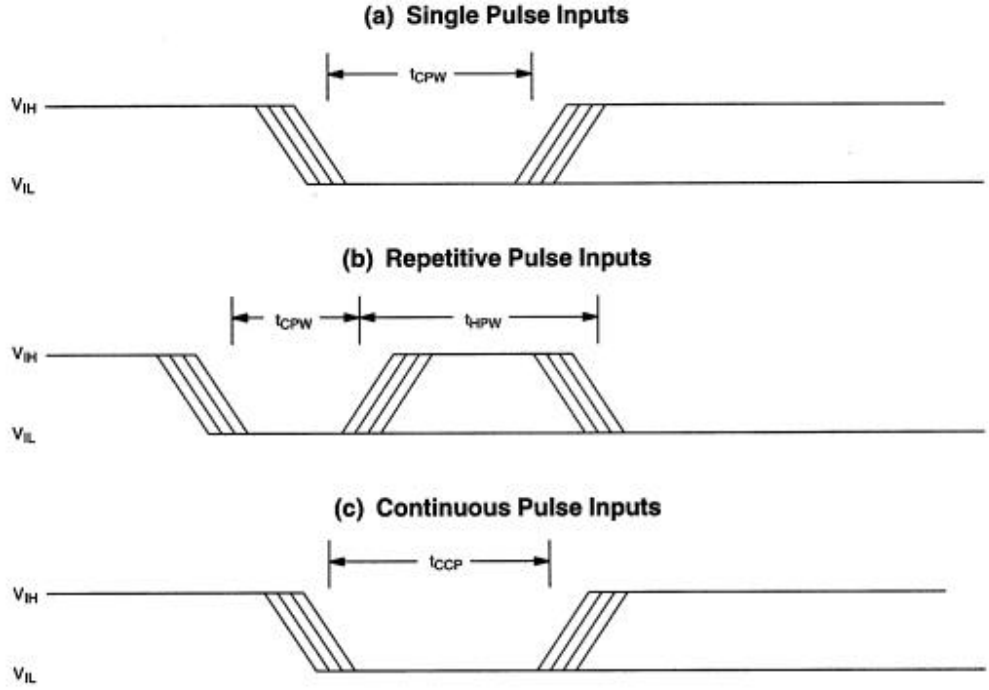
In stereo mode control, the VU input is responsible for both directions of wiper movement. Again, a period of inactivity will allow the direction of volume to be reversed. Additionally, if either wiper reaches a peak position, the direction of movement will automatically reverse.

For balance mode control, the B0 input will be responsible for wiper movement. A period of inactivity lasting 1 second or more will cause a switch in balance movement (i.e., balance-0 to balance-1).

DS1802 BALANCING EXAMPLE Figure 3



CONTACT CLOSURE TIMING (UC, DC) Figure 4



Dual Contact Closure

In dual pushbutton mode, each direction is controlled by the respective cont rol inputs. No wait states are required to change wiper direction, balance, or volume in dual pushbutton mode. Additionally, in dual pushbutton mode as the wiper position reaches the end of the potentiometer, the direction of wiper movement will not change. Wiper position will remain at the potentiometers' end until an opposite direction input is given.

All contact closure control inputs, UC0, UC1, DC0, DC1, VU, VD, B0 and B1 are internally pulled up by a 50 kO resistance. The UC0, UC1, DC0 DC1, VU, VD, B0, and B1 inputs are internally debounced and require no external components for input signal conditioning.

3-WIRE SERIAL INTERFACE CONTROL

One method of communication and control of the DS1802 is accomplished through a 3-wire serial port interface that drives an internal control logic unit. The 3-wire serial interface is designed for microprocessor or microcontroller applications. The interface consists of three input signals which include $\overline{RST}$, CLK and D.

The $\overline{RST}$ control signal is used to enable 3-wire serial port write operations. The CLK terminal is a clock signal input that provides synchronization for data I/O while the D signal input serves to transfer potentiometer wiper position settings to the device.

As shown in Figure 5, a 3-wire serial port operation begins with a transition of the $\overline{RST}$ signal input to a high state. Once the 3-wire port has been activated, data is clocked into the part on the low to high transition of the CLK signal input. Data input via the D line is transferred in order of the desired potentiometer-0 value followed by the potentiometer-1 value.

The DS1802 contains two 65-position potentiometers whose wiper positions are set by an 8-bit value. These two 8-bit values are written to the 16-bit I/O shift register which is used to store wiper position during powered conditions. Because the potentiometer has 65-positions, only seven bits of data are needed to set wiper position. A detailed diagram of the 16-bit I/O shift register is shown in Figure 5. Bits 0 through 7 are reserved for the potentiometer-0 control while bits 8 through 15 are reserved for control of potentiometer-1.

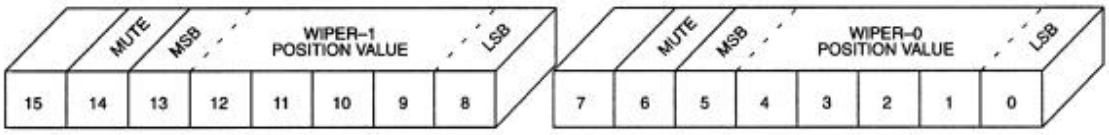
Bits 0 through 5 are used for actual wiper positioning for potentiometer-0. Bit 6 is used to mute potentiometer-0. If this bit has value 1, the potentiometer-0 wiper will be connected to the low end of the resistive array. The mute feature of the DS1802 will be discussed in the section entitled “Mute Operation of DS1802.” The value of bit 7 is a "don’t care" and will not affect operation of the DS1802 or potentiometer-0.

Bits 8 through 13 are used for wiper positioning of potentiometer-1. Bit 14 is used for muting of the potentiometer-1 wiper output. Bit 15, like bit 7, is a "don’t care" and will not affect operation of the DS1802.

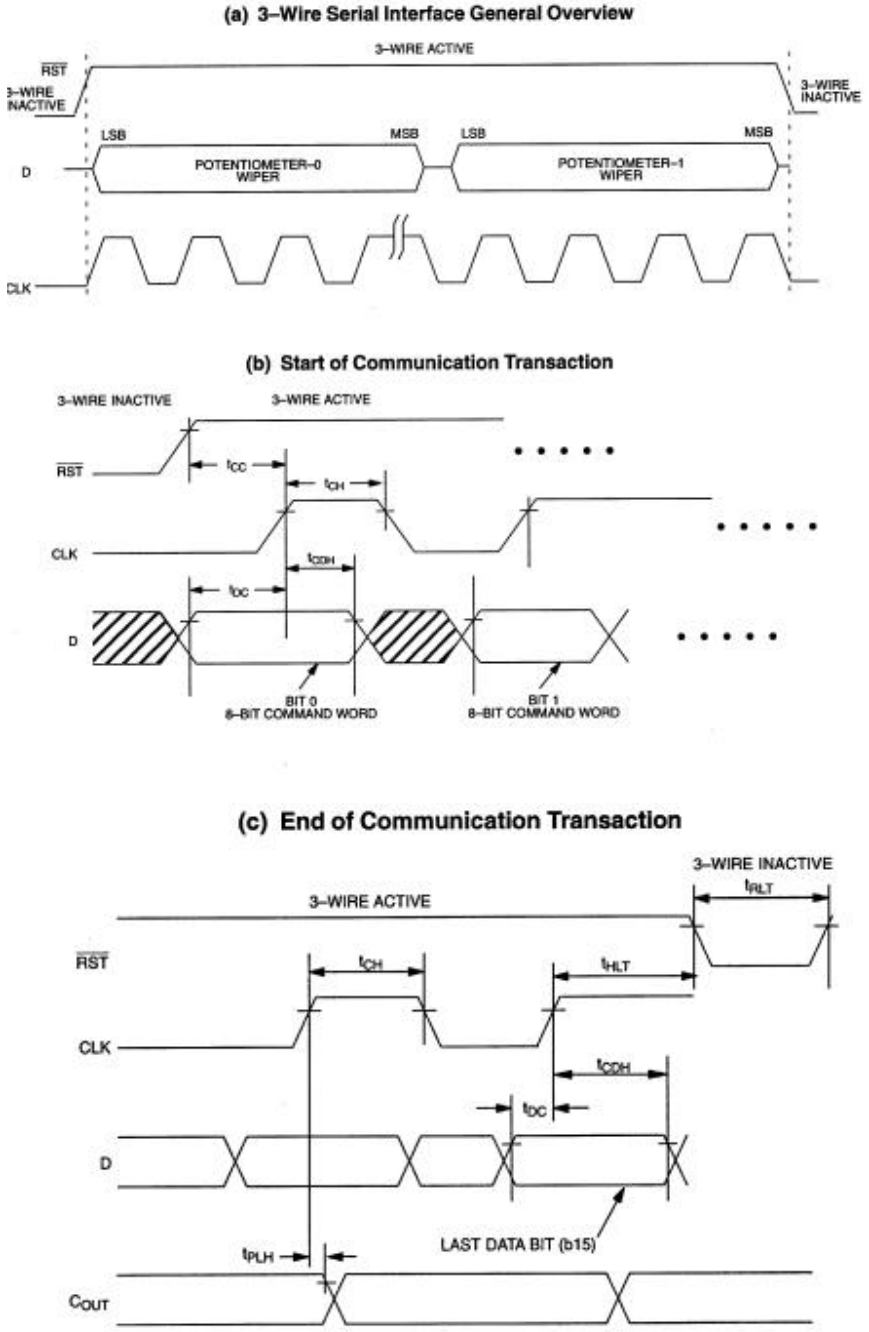
Data for the DS1802 is transmitted LSB first starting with bit 0. A complete transmission of 16 bits of data is required to insure proper setting of each potentiometer’s wiper. An incomplete transmission may result in undesired wiper settings.

Once the complete 16 bits of information has been transmitted and the $\overline{RST}$ signal input transitions to a low state, the new wiper positions are loaded into the part.

16-BIT I/O SHIFT REGISTER Figure 5



TIMING DIAGRAMS Figure 6



CASCADE OPERATION

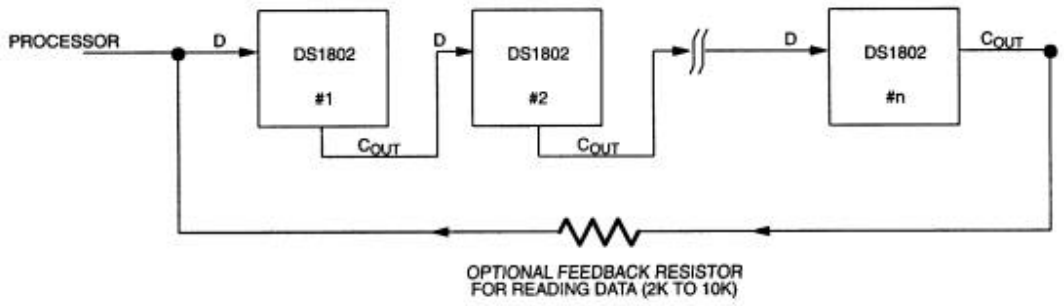
A feature of the DS1802 is the ability to control multiple devices from a single processor. Multiple DS1802s can be linked or daisy-chained as shown in Figure 7. As a bit is entered in to the I/O shift registeroftheDS1802 it will appear at the C_{OUT} out put after a maximum delay of 50 nanoseconds.

The C_{OUT} output of the DS1802 can be used to drive the D input of another DS1802. When connecting multiple devices, the total number of bits sent is always 16 times the number of DS1802s in the daisy chain.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the D input of the first DS1802, thus allowing the controlling processor to circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 2 kΩ to 10 kΩ.

When reading data via the C_{OUT} pin and isolation resistor, the D line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 0 is present on the C_{OUT} pin, which is fed back to the input D pin through the isolation resistor. When the CLK input transitions low to high, bit 0 is loaded into the first position of the I/O shift register and bit 1 becomes present on C_{OUT} and D of the next device. After 16 bits (or 16 times the number of DS1802s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded into the wiper-0 and wiper-1.

CASCADING MULTIPLE DEVICES Figure 7



Zero-Crossing Detection

The DS1802 provides a zero-crossing detection capability when using the 3-Wire Serial interface. Zero- crossing detection provides a means for minimizing any audible noise that may result from sizable discrete wiper transitions when using the part in audio applications. The zero-crossing detect feature allows independent wiper changes only when the two terminals of the potentiometer have equal potentials and within a 50 ms time window from the fall of the $\overline{RST}$ signal. If at 50 ms the DS1802 has not detected a zero-crossing, the wiper position of the potentiometer(s) will change regardless of the state of the input signal. Zero-crossing detection is activated when the $\overline{ZCEN}$ input level is in a low state. When high, the $\overline{ZCEN}$ input deactivates both the 50 ms time requirement and zero-crossing detection.

Zero-crossing detection is also available when using the part in pushbutton operation. When a pushbutton is activated, the part will change wiper position during the first detected zero-crossing or at the end of a 50 ms time window.

When operating in pushbutton operation with a continuous input pulse, the wiper position will change once during the initial 1-second time period. This change is dictated by a detected zero-crossing or 50 ms

time window. Subsequent changes when operating with continuous input pulse occur on 100 ms time intervals and are dependent on zero-crossing or 50 ms timeouts.

MUTE CONTROL

The DS1802 provides a mute control feature which can be accessed by the user through hardware or software. Hardware control of the device is achieved through the MUTE input pin. This pin is internally pulled up through a 50 kΩ resistor. When this input is driven low, the wiper outputs of both potentiometers will be internally connected to the low terminal of their respective potentiometers. This input performs as a toggle input, with the first activity on this pin connecting the wiper outputs to the low end of the resistive array on each potentiometer. The next input activity on this pin will return the wiper position to the previous state before the muting occurred. Also, if operating in pushbutton mode, mute will be deactivated if an input is received over the VU, VD, UC0, UC1, DC0, DC1 inputs. This input, like the pushbutton inputs, is internally debounced and requires no external circuitry. When the device powers up, the first activity on the mute pin will internally connect the wipers to the low end of the resistor array.

Software mute control was briefly discussed in 3-wire protocol and operation. Bits 6 and 14 of the 16-bit I/O shift register are reserved for mute control of potentiometer-0 and potentiometer-1, respectively. Unlike hardware mute control, software muting allows the user individual control of each potentiometer (i.e., potentiometer-0 and potentiometer-1 can be independently muted). Software muting of potentiometer-0 would require bit 6 to have a value of 1 while for potentiometer-1, bit 14 should have a value 1. When the user desires to release the mute of any potentiometer through software the complete 16-bit I/O shift register must be rewritten with the desired potentiometer wiper settings and bits 6 and 14 having 0 value.

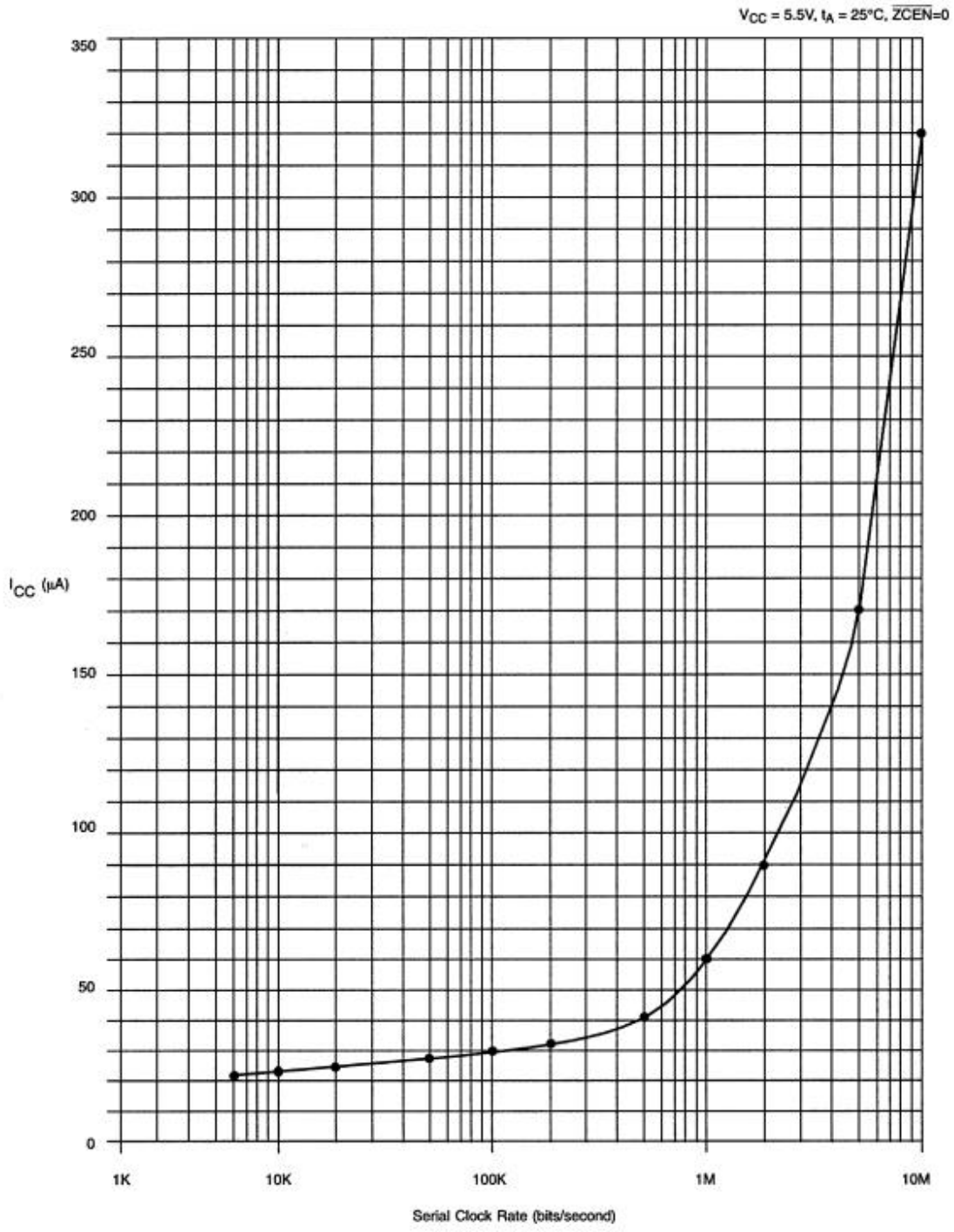
3-Wire Serial Port Vs. Pushbutton Operation

In applications where both the 3-wire serial port and the pushbutton inputs will be used to control the part, there may be times when activity is present on both control interfaces simultaneously. This section describes how the DS1802 handles these situations.

In all instances, the DS1802 3-wire serial port takes precedence over pushbutton input control.

The DS1802 will not allow pushbutton inputs to change wiper position during 3-wire serial port activity.

TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 8



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.7V to +7.0V
Operating Temperature	-40° to +85°C Storage
Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1,2
Input Logic 0	V_{IL}	-0.5		+0.8	V	1,2
Resistor Inputs	L,H,W	GND-0.5		V_{CC}+0.5	V	2
Analog Ground	AGND	GND-0.5		GND+0.5	V	14

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			2000	µA	12
Input Leakage	I_{LI}	-1		+1	µA	3
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Logic 1 Output Current @2.4V	I_{OH}	-1.0			mA	2
Logic 0 Output Current @0.4V	I_{OL}			4	mA	2
Standby Current: 3 Volts			22		µA	15
5 Volts			42	80	µA	
Power-Up Time	t_{PU}		50		ms	9

ANALOG RESISTOR CHARACTERISTICS (-40°C to +85°C;V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End to End Resistor Tolerance		-20		+20	%	17
Absolute Tolerance		-1		+1	dB	11
Inter-channel Matching		-0.5		+0.5	dB	6
Tap-to-Tap Tolerance		-0.25		+0.25	dB	7,16
-3 dB Cutoff Frequency	f_{CUTOFF}		700 kHz		kHz	
Temperature Coefficient			750		ppm/°C	
Total Harmonic Distortion (V_{IN}=1V_{RMS}, 1 kHz, Tap = -6 dB)	THD		0.002		%	16
Output Noise (20 Hz to 20 kHz, Grounded Input, Tap= -6 dB)			2.2		μV_{RMS}	
Digital Feedthrough (20 Hz to 20 kHz, Tap= -6 dB)			-90		dB	16
Interchannel Isolation (20 Hz to 20kHz, Tap= -6 dB)			-100		dB	16
Mute Control Active	Mute		-90		dB	

CAPACITANCE (-40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	8
Output Capacitance	C_{OUT}			7	pF	8

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	10,13
Width of CLK Pulse	t_{CH}	50			ns	10,13
Data Setup Time	t_{DC}	30			ns	10,13
Data Hold Time	t_{CDH}	10			ns	10,13
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	10,13
Propagation Delay Time Low to High Level	t_{PLH}			50	ns	10,13
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	10,13
$\overline{RST}$ Low to Clock Input High	t_{HLT}	50			ns	10,13
CLK Rise Time	t_{CR}			50	ns	10,13
$\overline{RST}$ Inactive	t_{RLT}	200			ns	10,13

AC ELECTRICAL CHARACTERISTICS (PUSHBUTTON INPUTS)

(-40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Single Pulse Input	t_{CPW}	1		DC	ms	3,5,13
Repetitive Input Pulse High Time	t_{HPW}	1		DC	ms	3,5,13
Continuous Input Pulse	t_{CCP}	1		DC	s	3,5,13

NOTES:

1. All voltages are referenced to ground.
2. Valid for V_{CC}=5V only.
3. Both UCx and DCx inputs are internally pulled up with a 50KΩ resistance.
4. Capacitance values apply at 25°C.
5. Input pulse width is the minimum time required for an input to cause an increment or decrement. If the UCx or DCx inputs is held active for longer than 1 second, subsequent increments or decrements will occur on 100 ms intervals until the inputs UCx, DCx are released to V_{IH}. Timing tolerances for pushbutton control is ±30%.
6. Inter-channel matching is used to determine the relative voltage difference in dB between the same tap position on each potentiometer. The DS1802 is specified for ±0.5 dB inter-channel matching.

7. Tap-to-tap tolerance is used to determine the change in voltage between successive tap positions. The DS1802 is specified for ±0.25 dB tap-to-tap tolerance.

8. Typical values are for t_A=25°C and nominal supply voltage.

9. Power-up time is the time for all pushbutton inputs to be stable and active once power has reached a valid level, 2.7V min.

10. See Figure 6.

11. Absolute tolerance is used to determine measured wiper voltage vs. expected wiper voltage as determined by wiper position. The DS1802 is bounded by a ±1 dB absolute tolerance.

12. Maximum current specifications are based on clock rate, active zero-crossing detection, and pushbutton activation. See Figure 8 for clock rate vs. current specification.

13. Valid for V_{CC}=3V or 5V.

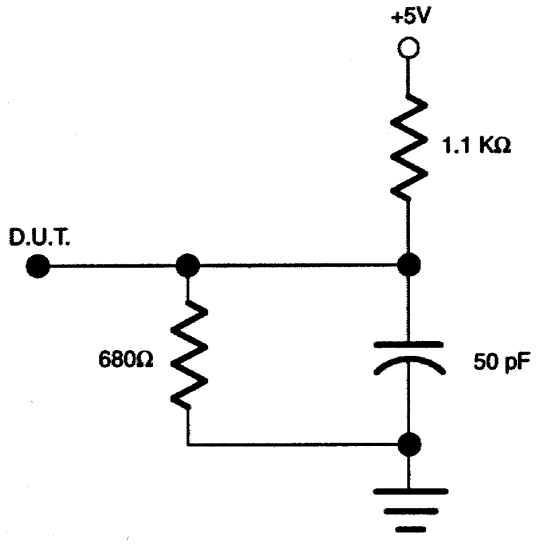
14. See Figure 10.

15. Standby current levels apply when all inputs are driven to appropriate supply levels.

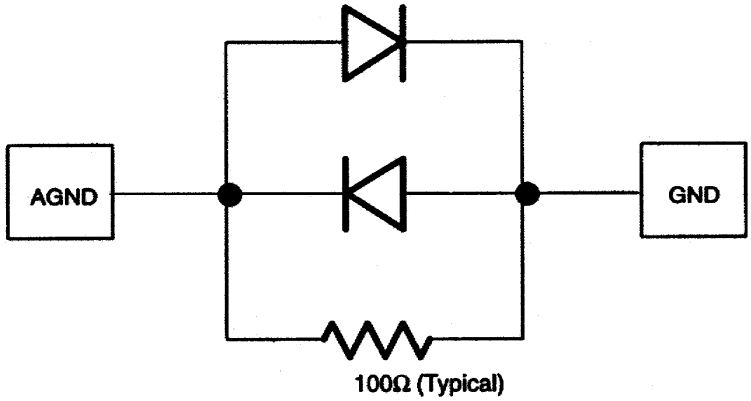
16. These parameters are characterized and not 100% tested.

17. Valid at 25°C only.

DIGITAL OUTPUT LOAD Figure 9



INTERNAL GROUND CONNECTIONS Figure 10



NOTE: GND and AGND must be tied to the same voltage level.

The FT232BL is the lead free version of the 2nd generation of FTDI's popular USB UART I.C. This device not only adds extra functionality to its FT8U232AM predecessor and reduces external component count, but also maintains a high degree of pin compatibility with the original, making it easy to upgrade or cost reduce existing designs as well as increasing the potential for using the device in new application areas.

1.0 Features

HARDWARE FEATURES

Single Chip USB ⇔Asynchronous Serial Data Transfer

Full Handshaking & Modem Interface Signals

UART I/F Supports 7 / 8 Bit Data, 1 / 2 Stop Bits and Odd/Even/Mark/Space/No Parity

Data rate 300 => 3M Baud (TTL)

Data rate 300 => 1M Baud (RS232)

Data rate 300 => 3M Baud (RS422/RS485)

384 Byte Receive Buffer / 128 Byte Transmit Buffer for high data throughput

Adjustable RX buffer timeout

Fully Assisted Hardware or X-On / X-Off Handshaking

In-built support for event characters and line break condition

Auto Transmit Buffer control for RS485

Support for USB Suspend / Resume through SLEEP# and RI# pins

Support for high power USB Bus powered devices through PWREN# pin

Integrated level converter on UART and control signals for interfacing to 5V and 3.3V logic

Integrated 3.3V regulator for USB IO

Integrated Power-On-Reset circuit

Integrated 6MHz – 48Mhz clock multiplier PLL

USB Bulk or Isochronous data transfer modes

4.35V to 5.25V single supply operation

UHCI / OHCI / EHCI host controller compatible

USB 1.1 and USB 2.0 compatible

USB VID, PID, Serial Number and Product Description strings in external EEPROM

EEPROM programmable on-board via USB

Compact Lead free RoHS compliant 32-LD LQFP package.

VIRTUAL COM PORT (VCP) DRIVERS for

- Windows 98 and Windows 98 SE
- Windows 2000 / ME / Server 2003 / XP
- Windows XP 64 Bit
- Windows XP Embedded
- Windows CE 4.2
- MAC OS-8 and OS-9
- MAC OS-X
- Linux 2.40 and greater

D2XX (USB Direct Drivers + DLL S/W Interface)

- Windows 98 and Windows 98 SE
- Windows 2000 / ME / Server 2003 / XP
- Windows XP 64 Bit
- Windows XP Embedded
- Windows CE 4.2
- Linux 2.40 and greater

APPLICATION AREAS

- USB ⇔RS232 Converters
- USB ⇔ RS422 / RS485 Converters
- Upgrading RS232 Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA ⇔ USB data transfer
- USB Smart Card Readers
- Set Top Box (S.T.B.) PC - USB interface
- USB Hardware Modems
- USB Wireless Modems
- USB Instrumentation
- USB Bar Code Readers

2.0 Enhancements

This section summarises the enhancements of the 2nd generation device compared to its FT8U232AM predecessor. For further details, consult the device pin-out description and functional descriptions.

Integrated Power-On-Reset (POR) Circuit

The device now incorporates an internal POR function. The existing RESET# pin is maintained in order to allow external logic to reset the device where required, however for many applications this pin can now simply be hard wired to VCC. In addition, a new reset output pin (RSTOUT#) is provided in order to allow the new POR circuit to provide a stable reset to external MCU and other devices. RSTOUT# was the TEST pin on the previous generation of devices.

Integrated RCCLK Circuit

In the previous devices, an external RC circuit was required to ensure that the oscillator and clock multiplier PLL frequency was stable prior to enabling the clock internal to the device. This circuit is now embedded on-chip – the pin assigned to this function is now designated as the TEST pin and should be tied to GND for normal operation.

Integrated Level Converter on UART interface and control signals

The previous devices would drive the UART and control signals at 5V CMOS logic levels. The new device has a separate VCC-IO pin allowing the device to directly interface to 3.3V and other logic families without the need for external level converter I.C.'s

Improved Power Management control for USB Bus Powered, high current devices

The previous devices had a USBEN pin, which became active when the device was enumerated by USB. To provide power control, this signal had to be externally gated with SLEEP# and RESET#. This gating is now done on-chip - USBEN has now been replaced with the new PWREN# signal which can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. A new EEPROM based option makes the device pull gently down its UART interface lines when the power is shut off (PWREN# is High). In this mode, any residual voltage on external circuitry is bled to GND when power is removed thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.

Lower Suspend Current

Integration of RCCLK within the device and internal design improvements reduce the suspend current of the FT232BL to under 200uA (excluding the 1.5k pull-up on USBDP) in USB suspend mode. This allows greater margin for peripherals to meet the USB Suspend current limit of 500uA.

Support for USB Isochronous Transfers

Whilst USB Bulk transfer is usually the best choice for data transfer, the scheduling time of the data is not guaranteed. For applications where scheduling latency takes priority over data integrity such as transferring audio and low bandwidth video data, the new device now offers an option of USB Isochronous transfer via an option bit in the EEPROM.

Programmable Receive Buffer Timeout

In the previous device, the receive buffer timeout used to flush remaining data from the receive buffer was fixed at 16ms timeout. This timeout is now programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be better optimised for protocols requiring faster response times from short data packets.

TXDEN Timing fix

TXDEN timing has now been fixed to remove the external delay that was previously required for RS485 applications at high baud rates. TXDEN now works correctly during a transmit send-break condition.

Relaxed VCC Decoupling

The 2nd generation devices now incorporate a level of on-chip VCC decoupling. Though this does not eliminate the need for external decoupling capacitors, it significantly improves the ease of PCB design requirements to meet FCC, CE and other EMI related specifications.

Improved PreScaler Granularity

The previous version of the Prescaler supported division by (n + 0), (n + 0.125), (n + 0.25) and (n + 0.5) where n is an integer between 2 and 16,384 (2^{14}). To this we have added (n + 0.375), (n + 0.625), (n + 0.75) and (n+ 0.875) which can be used to improve the accuracy of some baud rates and generate new baud rates which were previously impossible (especially with higher baud rates).

Bit Bang Mode

The 2nd generation device has a new option referred to as “Bit Bang” mode. In Bit Bang mode, the eight UART interface control lines can be switched between UART interface mode and an 8-bit Parallel IO port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by the prescaler setting. As well as allowing the device to be used stand-alone as a general purpose IO controller for example controlling lights, relays and switches, some other interesting possibilities exist. For instance, it may be possible to connect the device to an SRAM configurable FPGA as supplied by vendors such as Altera and Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use Bit Bang Mode to download configuration data to the FPGA which would define its hardware function, then after the FPGA device is configured the FT232BL can switch back into UART interface mode to allow the programmed FPGA device to communicate with the PC over USB. This approach allows a customer to create a “generic” USB peripheral who’s hardware function can be defined under control of the application software. The FPGA based hardware can be easily upgraded or totally changed simply by changing the FPGA configuration data file. Application notes, software and development modules for this application area will be available from FTDI and other 3rd parties.

PreScaler Divide By 1 Fix

The previous device had a problem when the integer part of the divisor was set to 1. In the 2nd generation device setting the prescaler value to 1 gives a baud rate of 2 million baud and setting it to zero gives a baud rate of 3 million baud. Non-integer division is not supported with divisor values of 0 and 1.

Less External Support Components

As well as eliminating the RCCLK RC network, and for most applications the need for an external reset circuit, we have also eliminated the requirement for a 100K pull-up on EECS to select 6MHz operation. When the FT232BL is being used without the configuration EEPROM, EECS, EESK and EEDATA can now be left n/c. For circuits requiring a long reset time (where the device is reset externally using a reset generator I.C., or reset is controlled by the IO port of a MCU, FPGA or ASIC device) an external transistor circuit is no longer required as the 1.5k pull-up resistor on USBDP can be wired to the RSTOUT# pin instead of to 3.3V. Note : RSTOUT# drives out at 3.3V level, not at 5V VCC level. This is the preferred configuration for new designs.

Extended EEPROM Support

The previous generation of devices only supported EEPROM of type 93C46 (64 x 16 bit). The new devices will also work with EEPROM type 93C56 (128 x 16 bit) and 93C66 (256 x 16 bit). The extra space is not used by the device, however it is available for use by other external MCU / logic whilst the FT232BL is being held in reset.

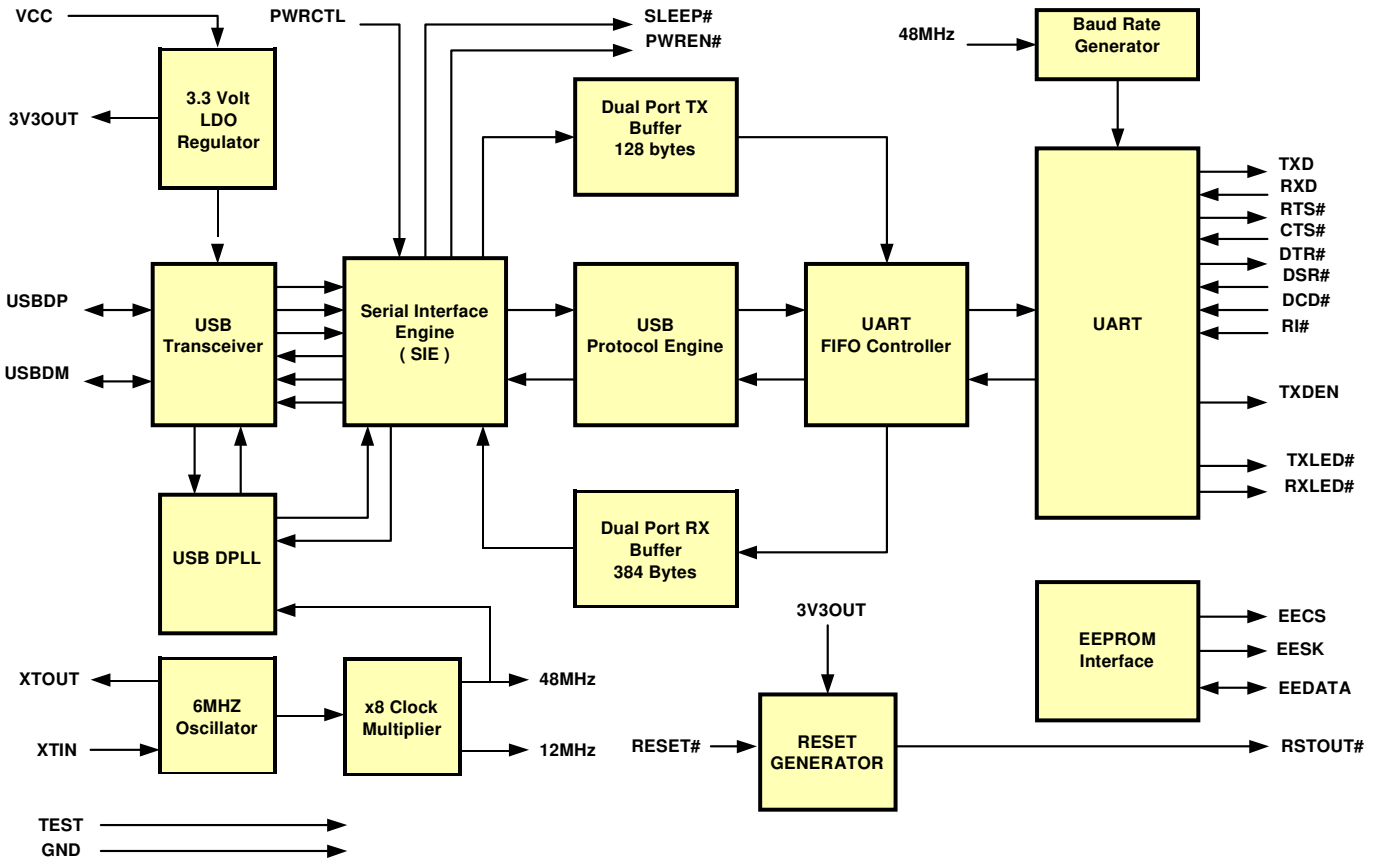
USB 2.0 (full speed option)

A new EEPROM based option allows the FT232BL to return a USB 2.0 device descriptor as opposed to USB 1.1. Note : The device would be a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).

Multiple Device Support without EEPROM

When no EEPROM (or a blank or invalid EEPROM) is attached to the device, the FT232BL no longer gives a serial number as part of its USB descriptor. This allows multiple devices to be simultaneously connected to the same PC. However, we still highly recommend that EEPROM is used, as without serial numbers a device can only be identified by which hub port in the USB tree it is connected to which can change if the end user re-plugs the device into a different port.

3.0 Block Diagram (Simplified)



3.1 Functional Block Descriptions

3.3V LDO Regulator

The 3.3V LDO Regulator generates the 3.3 volt reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides 3.3V power to the RSTOUT# pin. The main function of this block is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, external circuitry requiring 3.3V nominal at a current of not greater than 5mA could also draw its power from the 3V3OUT pin if required.

USB Transceiver

The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide 3.3 volt level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB data in, SEO and USB Reset condition detection.

USB DPLL

The USB DPLL cell locks on to the incoming NRZI USB data and provides separate recovered clock and data signals to the SIE block.

6MHz Oscillator

The 6MHz Oscillator cell generates a 6MHz reference clock input to the x8 Clock multiplier from an external 6MHz crystal or ceramic resonator.

x8 Clock Multiplier

The x8 Clock Multiplier takes the 6MHz input from the Oscillator cell and generates a 12MHz reference clock for the SIE, USB Protocol Engine and UART FIFO controller blocks. It also generates a 48MHz reference clock for the USB DPPL and the Baud Rate Generator blocks.

Serial Interface Engine (SIE)

The Serial Interface Engine (SIE) block performs the Parallel to Serial and Serial to Parallel conversion of the USB data. In accordance to the USB 2.0 specification, it performs bit stuffing / un-stuffing and CRC5 / CRC16 generation / checking on the USB data stream.

USB Protocol Engine

The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol (Chapter 9) requests generated by the USB host controller and the commands for controlling the functional parameters of the UART.

Dual Port TX Buffer (128 bytes)

Data from the USB data out endpoint is stored in the Dual Port TX buffer and removed from the buffer to the UART transmit register under control of the UART FIFO controller.

Dual Port RX Buffer (384 bytes)

Data from the UART receive register is stored in the Dual Port RX buffer prior to being removed by the SIE on a USB request for data from the device data in endpoint.

UART FIFO Controller

The UART FIFO controller handles the transfer of data between the Dual Port RX and TX buffers and the UART transmit and receive registers.

UART

The UART performs asynchronous 7 / 8 bit Parallel to Serial and Serial to Parallel conversion of the data on the RS232 (RS422 and RS485) interface. Control signals supported by the UART include RTS, CTS, DSR , DTR, DCD and RI. The UART provides a transmitter enable control signal (TXDEN) to assist with interfacing to RS485 transceivers. The UART supports RTS/ CTS, DSR/DTR and X-On/X-Off handshaking options. Handshaking, where required, is handled in hardware to ensure fast response times. The UART also supports the RS232 BREAK setting and detection conditions.

Baud Rate Generator

The Baud Rate Generator provides a x16 clock input to the UART from the 48MHz reference clock and consists of a 14 bit prescaler and 3 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 3 million baud.

RESET Generator

The Reset Generator Cell provides a reliable power-on reset to the device internal circuitry on power up. An additional RESET# input and RSTOUT# output are provided to allow other devices to reset the FT232BL or the FT232BL to reset other devices respectively. During reset, RSTOUT# is driven low, otherwise it drives out at the 3.3V provided by the onboard regulator. RSTOUT# can be used to control the 1.5k pull-up on USBDP directly where delayed USB enumeration is required. It can also be used to reset other devices. RSTOUT# will stay high-impedance for approximately 5ms after VCC has risen above 3.5V AND the device oscillator is running AND RESET# is high. RESET# should be tied to VCC unless it is a requirement to reset the device from external logic or an external reset generator i.c.

EEPROM Interface

Though the FT232BL will work without the optional EEPROM, an external 93C46 (93C56 or 93C66) EEPROM can be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT232BL for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Isochronous Transfer Mode, Soft Pull Down on Power-Off and USB 2.0 descriptor modes.

The EEPROM should be a 16 bit wide configuration such as a MicroChip 93LC46B or equivalent capable of a 1Mb/s clock rate at VCC = 4.35V to 5.25V. The EEPROM is programmable-on board over USB using a utility available from FTDI's web site (http://www.ftdichip.com). This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process.

If no EEPROM is connected (or the EEPROM is blank), the FT232BL will use its built-in default VID, PID Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

4.0 Device Pin-Out

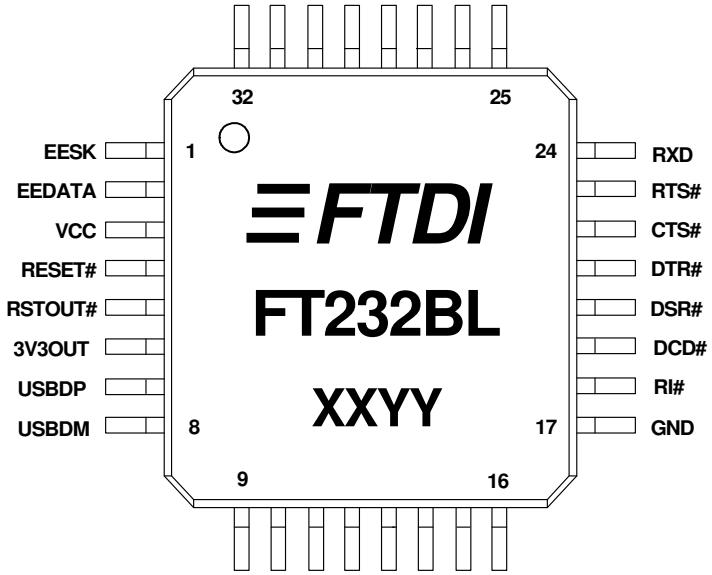


Figure 1
Pin-Out
(Lead free LQFP-32 Package)

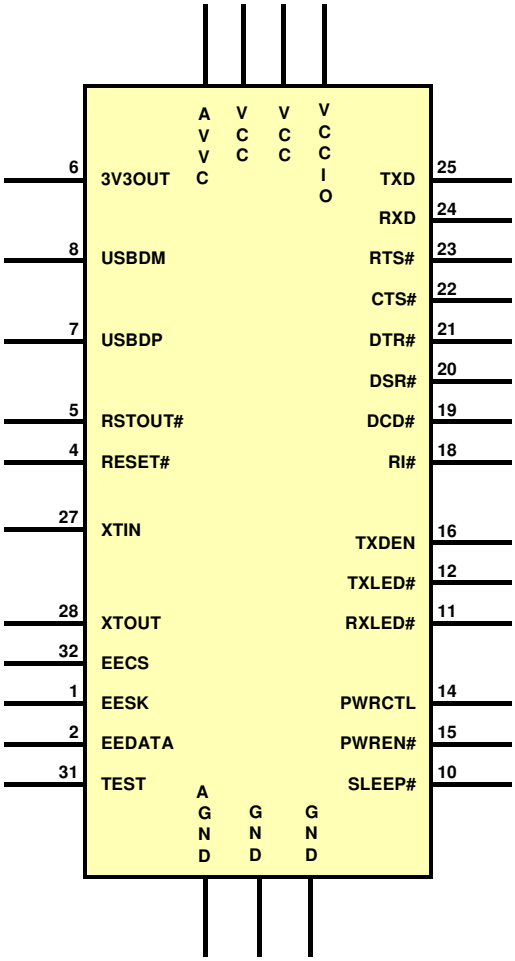


Figure 2
Pin-Out
(Schematic Symbol)

4.1 Signal Descriptions

Table 1 - FT232BL - PINOUT DESCRIPTION

UART INTERFACE GROUP

Pin#	Signal	Type	Description
25	TXD	OUT	Transmit Asynchronous Data Output
24	RXD	IN	Receive Asynchronous Data Input
23	RTS#	OUT	Request To Send Control Output / Handshake signal
22	CTS#	IN	Clear To Send Control Input / Handshake signal
21	DTR#	OUT	Data Terminal Ready Control Output / Handshake signal
20	DSR#	IN	Data Set Ready Control Input / Handshake signal
19	DCD#	IN	Data Carrier Detect Control Input
18	RI#	IN	Ring Indicator Control Input. When the Remote Wakeup option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend.
16	TXDEN	OUT	Enable Transmit Data for RS485

USB INTERFACE GROUP

Pin#	Signal	Type	Description
7	USBDP	I/O	USB Data Signal Plus (Requires 1.5k pull-up to 3V3OUT or RSTOUT#)
8	USBDM	I/O	USB Data Signal Minus

EEPROM INTERFACE GROUP

Pin#	Signal	Type	Description
32	EECS	I/O	EEPROM – Chip Select. For 48MHz operation pull EECS to GND using a 10K resistor. For 6MHz operation no resistor is required. Tri-State during device reset. **Note 1
1	EESK	OUT	Clock signal to EEPROM. Tri-State during device reset, else drives out. Adding a 10K pull down resistor onto EESK will cause the FT232BL to use USB Product ID 6004 (hex) instead of 6001 (hex). All of the other USB device descriptors are unchanged.**Note 1
2	EEDATA	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset. **Note 1

POWER CONTROL GROUP

Pin#	Signal	Type	Description
10	SLEEP#	OUT	Goes Low during USB Suspend Mode. Typically used to power-down an external TTL to RS232 level converter i.c. in USB <=> RS232 converter designs.
15	PWREN#	OUT	Goes Low after the device is configured via USB, then high during USB suspend. Can be used to control power to external logic using a P-Channel Logic Level MOSFET switch. Enable the Interface Pull-Down Option in EEPROM when using the PWREN# pin in this way.
14	PWRCTL	IN	Bus Powered – Tie Low / Self Powered – Tie High (to VCCIO)

MISCELLANEOUS SIGNAL GROUP

Pin#	Signal	Type	Description
4	RESET#	IN	Can be used by an external device to reset the FT232BL. If not required, tie to VCC.
5	RSTOUT#	OUT	Output of the internal Reset Generator. Stays high impedance for ~ 5ms after VCC > 3.5V and the internal clock starts up, then clamps its output to the 3.3v output of the internal regulator. Taking RESET# low will also force RSTOUT# to drive low. RSTOUT# is NOT affected by a USB Bus Reset.
12	TXLED#	O.C.	LED Drive - Pulses Low when Transmitting Data via USB
11	RXLED#	O.C.	LED Drive - Pulses Low when Receiving Data via USB
27	XTIN	IN	Input to 6MHz Crystal Oscillator Cell. This pin can also be driven by an external 6MHz clock if required. Note : Switching threshold of this pin is VCC/2, so if driving from an external source, the source must be driving at 5V CMOS level or a.c. coupled to centre around VCC/2.
28	XTOUT	OUT	Output from 6MHz Crystal Oscillator Cell. XTOUT stops oscillating during USB suspend, so take care if using this signal to clock external logic.
31	TEST	IN	Puts device in I.C. test mode – must be tied to GND for normal operation.

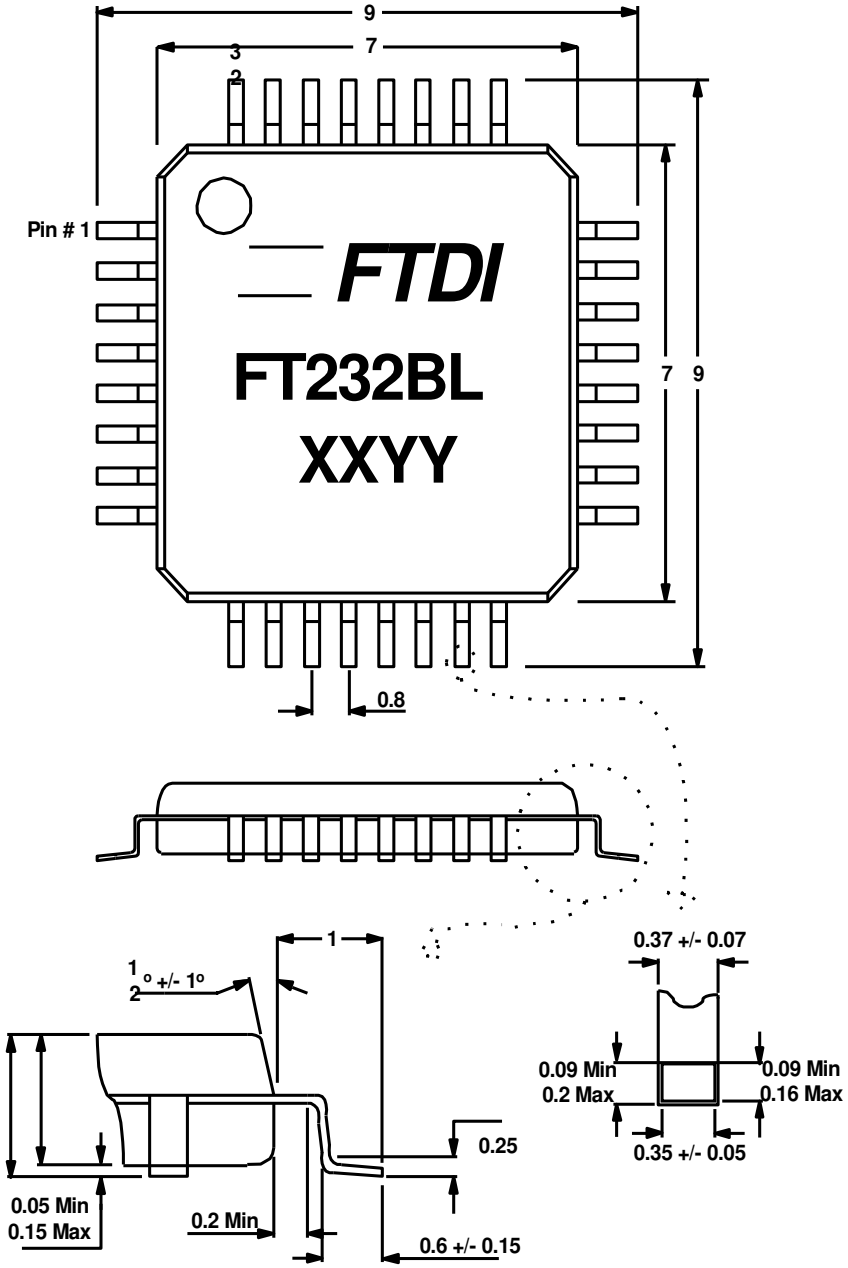
POWER AND GND GROUP

Pin#	Signal	Type	Description
6	3V3OUT	OUT	3.3 volt Output from the integrated L.D.O. regulator This pin should be decoupled to GND using a 33nF ceramic capacitor in close proximity to the device pin. Its prime purpose is to provide the internal 3.3V supply to the USB transceiver cell and the RSTOUT# pin. A small amount of current (<= 5mA) can be drawn from this pin to power external 3.3v logic if required.
3,26	VCC	PWR	+4.35 volt to +5.25 volt VCC to the device core, LDO and non-UART interface pins.
13	VCCIO	PWR	+3.0 volt to +5.25 volt VCC to the UART interface pins 10..12, 14..16 and 18..25. When interfacing with 3.3V external logic in a bus powered design connect VCCIO to a 3.3V supply generated from the USB bus. When interfacing with 3.3V external logic in a self powered design connect VCCIO to the 3.3V supply of the external logic. Otherwise connect to VCC to drive out at 5V CMOS level.
9,17	GND	PWR	Device - Ground Supply Pins
30	AVCC	PWR	Device - Analog Power Supply for the internal x8 clock multiplier
29	AGND	PWR	Device - Analog Ground Supply for the internal x8 clock multiplier

****Note 1 -** During device reset, these pins are tri-state but pulled up to VCC via internal 200K resistors.

5.0 Package Outline

Figure 3 – 32 LD Lead Free LQFP Package Dimensions



The FT232BL is supplied in a 32 pin lead free LQFP package. This package has a 7mm x 7mm body (9mm x 9mm including leads) with leads on a 0.8mm pitch. The above drawing shows the LQFP-32 package – all dimensions are in millimetres. Note that there are two date code formats used - XXYY = Date Code where XX = 2 digit year number, YY = 2 digit week number; or XYY-1 where X = 1 digit year. number, YY = 2 digit week number.

The FT232BL is fully compliant with the European Union RoHS directive.

An alternative 5mm x 5mm leadless QFN32 package is also available for projects where package area is critical. Part numeber for this version is FT232BQ. The FT232BQ is also a lead free package. See their seperate datasheets for package dimensions.

6.0 Absolute Maximum Ratings

These are the absolute maximum ratings for the FT232BL device in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Units
Storage Temperature	–65°C to + 150°C	Degrees C
Floor Life (Out of Bag) at Factory Ambient (30°C/60% Relative Humidity)	192 Hours (Level 3 Compliant) **Note 2	
Ambient Temperature (Power Applied)	0°C to + 70°C	Degrees C
M.T.B.F. (at 35°C)	247484 Hours ≈ 28 Years	
VCC Supply Voltage	-0.5 to +6.00	V
D.C. Input Voltage - USBDP and USBDM	-0.5 to +3.8	V
D.C. Input Voltage - High Impedance Bidirectionals	-0.5 to +(Vcc +0.5)	V
D.C. Input Voltage - All other Inputs	-0.5 to +(Vcc +0.5)	V
DC Output Current – Outputs	24	mA
DC Output Current – Low Impedance Bidirectionals	24	mA
Power Dissipation (VCC = 5.25V)	500	mW
Electrostatic Discharge Voltage (Human Body Model) (I < 1uA)	+/- 3000	V
Latch Up Current (Vi = +/- 10V maximum, for 10 ms)	+/-200	mA

**Note 2 – *If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of 110°C and baked for 8 to 10 hours.*

6.1 D.C. Characteristics

DC Characteristics (Ambient Temperature = 0 to 70°C)

Operating Voltage and Current

Parameter	Description	Min	Typ	Max	Units	Conditions
Vcc1	VCC Operating Supply Voltage	4.35	5.0	5.25	V	
Vcc2	VCCIO Operating Supply Voltage	3.0	-	5.25	V	
Icc1	Operating Supply Current	-	25	-	mA	Normal Operation
Icc2	Operating Supply Current	-	180	200	uA	USB Suspend **Note 3

**Note 3 – *Supply current excludes the 200uA nominal drawn by the external pull-up resistor on USBDP.*

UART IO Pin Characteristics (VCCIO = 5.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	**Note 4
VHys	Input Switching Hysteresis	50	55	60	mV	

UART IO Pin Characteristics (VCCIO = 3.0 - 3.6V)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2 mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**Note 4
VHys	Input Switching Hysteresis	20	25	30	mV	

**Note 4 – *Inputs have an internal 200K pull-up resistor to VCCIO.*

XTIN / XTOUT Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	4.0	-	5.0	V	Fosc = 6MHz
Vol	Output Voltage Low	0.1	-	1.0	V	Fosc = 6MHz
Vin	Input Switching Threshold	1.8	2.5	3.2	V	

RESET#, TEST, EECS, EESK, EEDATA Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2 mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	**Note 5
VHys	Input Switching Hysteresis	50	55	60	mV	

**Note 5 – *EECS, EESK and EEDATA pins have an internal 200K pull-up resistor to VCC*

RSTOUT Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.0	-	3.6	V	I source = 2mA
Vol	Output Voltage Low	0.3	-	0.6	V	I sink = 2mA

USB IO Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
UVoh	IO Pins Static Output (High)	2.8		3.6	V	RI = 1.5K to 3V3Out (D+) RI = 15K to GND (D-)
UVol	IO Pins Static Output (Low)	0		0.3	V	RI = 1.5K to 3V3Out (D+) RI = 15K to GND (D-)
UVse	Single Ended Rx Threshold	0.8		2.0	V	
UCom	Differential Common Mode	0.8		2.5	V	
UVDif	Differential Input Sensitivity	0.2			V	
UDrvZ	Driver Output Impedance	29		44	Ohm	**Note 5

**Note 5 – *Driver Output Impedance includes the external 27R series resistors on USBDP and USBDM pins.*

7.0 Device Configuration Examples

7.1 Oscillator Configurations

Figure 4
3-Pin Ceramic Resonator Configuration

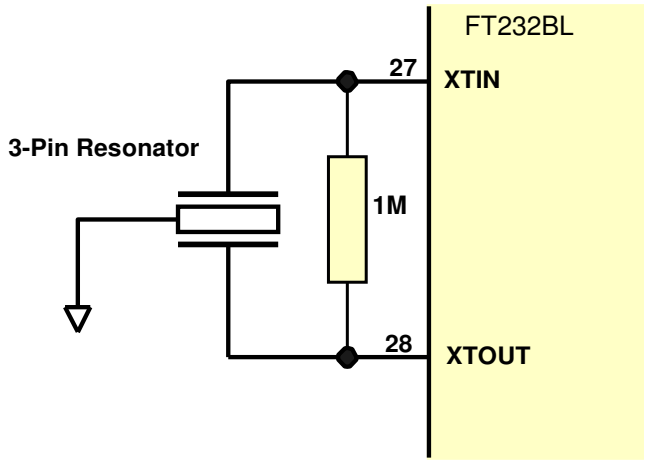


Figure 5
Crystal or 2-Pin Ceramic Resonator Configuration

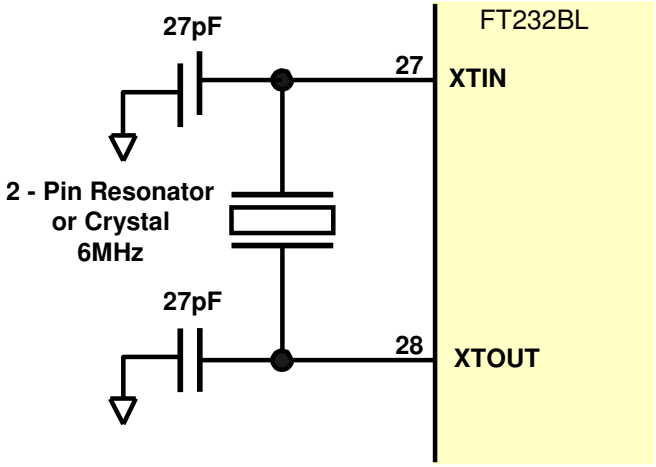


Figure 4 illustrates how to use the FT232BL with a 3-Pin Ceramic Resonator. A suitable part would be a ceramic resonator from Murata's CERALOCK range. (Murata Part Number CSTCR6M00G15), or equivalent. 3-Pin ceramic resonators have the load capacitors built into the resonator so no external loading capacitors are required. This makes for an economical configuration. The accuracy of this Murata ceramic resonator is +/- 0.1% and it is specifically designed for USB full speed applications. A 1 MegaOhm loading resistor across XTIN and XTOUT is recommended in order to guarantee this level of accuracy.

Other ceramic resonators with a lesser degree of accuracy (typically +/- 0.5%) are technically out-with the USB specification, but it has been calculated that using such a device will work satisfactorily in practice with a FT232BL design.

Figure 5 illustrates how to use the FT232BL with a 6MHz Crystal or 2-Pin Ceramic Resonator. In this case, these devices do not have in-built loading capacitors so these have to be added between XTIN, XTOUT and GND as shown. A value of 27pF is shown as the capacitor in the example – this will be good for many crystals and some resonators but do select the value based on the manufacturers recommendations wherever possible. If using a crystal, use a parallel cut type. If using a resonator, see the previous note on frequency accuracy.

7.2 EEPROM Configuration

Figure 6
EEPROM Configuration

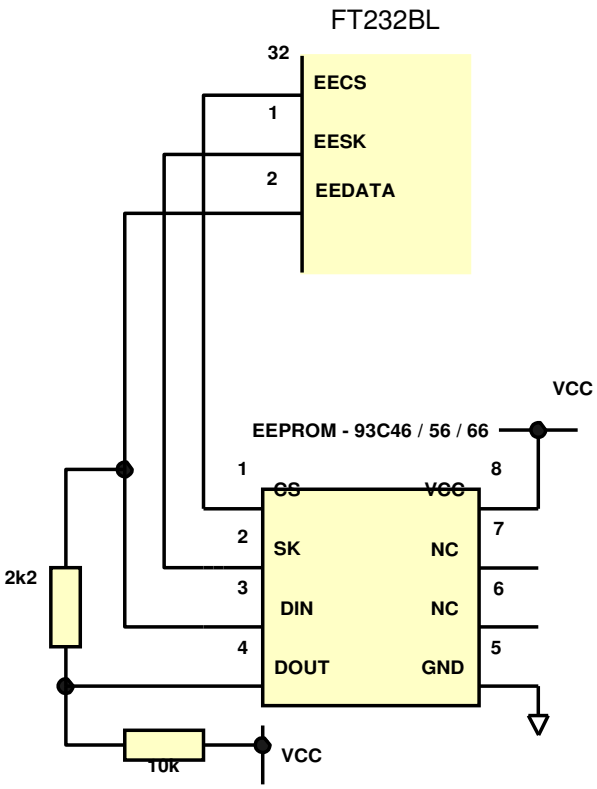


Figure 6 illustrates how to connect the FT232BL to the 93C46 (93C56 or 93C66) EEPROM. EECS (pin 32) is directly connected to the chip select (CS) pin of the EEPROM. EESK (pin 1) is directly connected to the clock (SK) pin of the EEPROM. EEDATA (pin 2) is directly connected to the Data In (Din) pin of the EEPROM. There is a potential condition whereby both the Data Output (Dout) of the EEPROM can drive out at the same time as the EEDATA pin of the FT232BL. To prevent potential data clash in this situation, the Dout of the EEPROM is connected to EEDATA of the FT232BL via a 2.2K resistor.

Following a power-on reset or a USB reset, the FT232BL will scan the EEPROM to find out (a) if an EEPROM is attached to the Device and (b) if the data in the device is valid. If both of these are the case, then the FT232BL will use the data in the EEPROM, otherwise it will use its built-in default values. When a valid command is issued to the EEPROM from the FT232BL, the EEPROM will acknowledge the command by pulling its Dout pin low. In order to check for this condition, it is necessary to pull Dout high using a 10K resistor. If the command acknowledge doesn't happen then EEDATA will be pulled high by the 10K resistor during this part of the cycle and the device will detect an invalid command or no EEPROM present.

There are two varieties of these EEPROM's on the market – one is configured as being 16 bits wide, the other is configured as being 8 bits wide. These are available from many sources such as Microchip, STMicro, ISSI etc. The FT232BL requires EEPROM's with a 16-bit wide configuration such as the Microchip 93LC46B device. The EEPROM must be capable of reading data at a 1Mb clock rate at a supply voltage of 4.35V to 5.25V. Most available parts are capable of this.

Check the manufacturers data sheet to find out how to connect pins 6 and 7 of the EEPROM. Some devices specify these as no-connect, others use them for selecting 8 / 16 bit mode or for test functions. Some other parts have their pinout rotated by 90° so please select the required part and its options carefully.

It is possible to "share" the EEPROM between the FT232BL and another external device such as an MCU. However, this can only be done when the FT232BL is in its reset condition as it tri-states its EEPROM interface at that time. A typical configuration would use four bit's of an MCU IO Port. One bit would be used to hold the FT232BL reset (using RESET#) on power-up, the other three would connect to the EECS, EESK and EEDATA pins of the FT232BL in order to read / write data to the EEPROM at this time. Once the MCU has read / written the EEPROM, it would take RESET# high to allow the FT232BL to configure itself and enumerate over USB.

7.3 USB Bus Powered and Self Powered Configuration

Figure 7
USB Bus Powered Configuration

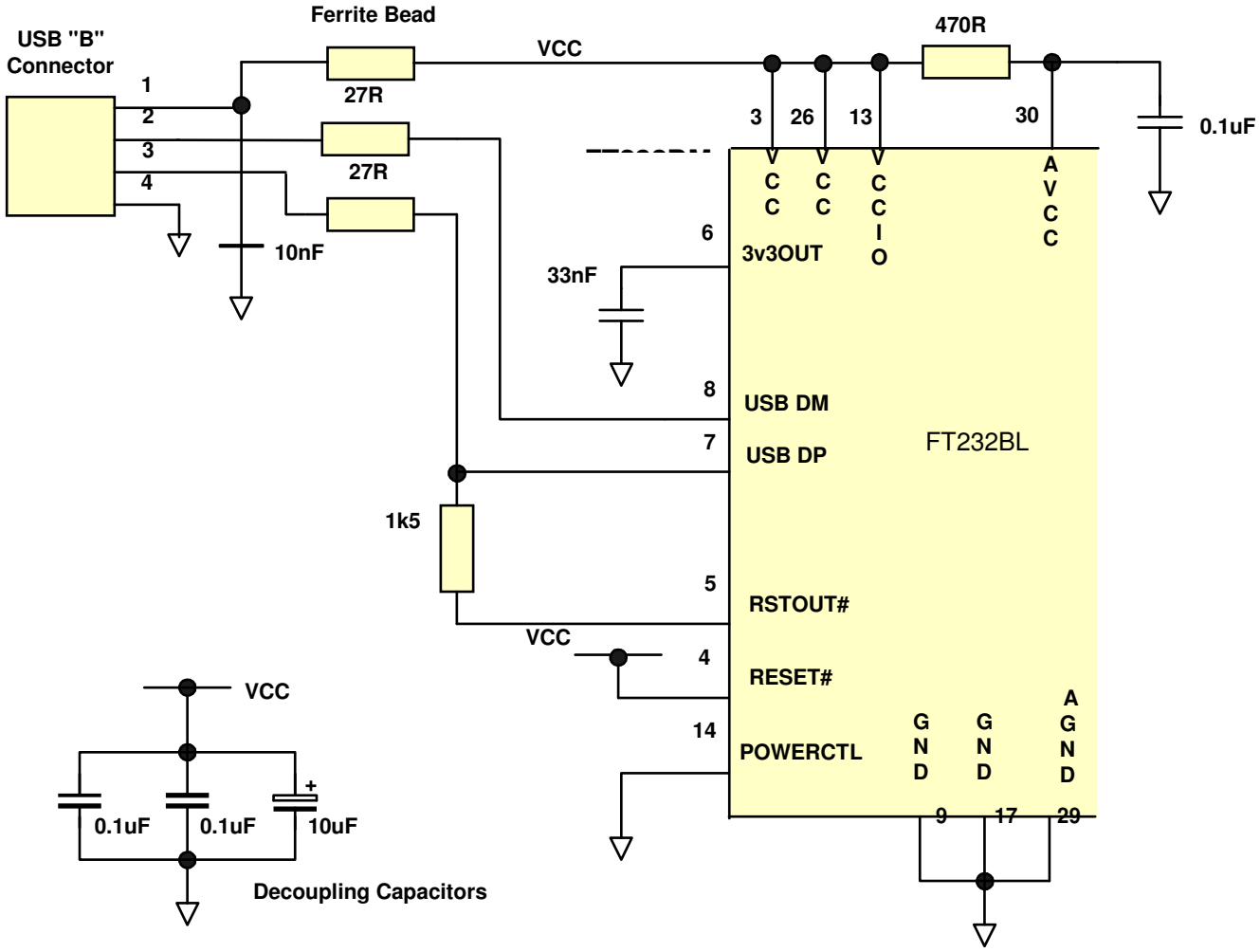


Figure 7 illustrates a typical USB bus powered configuration. A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows –

a) On plug-in, the device must draw no more than 100mA
b) On USB Suspend the device must draw no more than 500uA.
c) A Bus Powered High Power Device (one that draws more than 100mA) should use the PWREN# pin to keep the current below 100mA on plug-in and 500uA on USB suspend.
d) A device that consumes more than 100mA can not be plugged into a USB Bus Powered Hub
e) No device can draw more that 500mA from the USB Bus.

PWRCTL (pin 14) is pulled low to tell the device to use a USB Bus Power descriptor. The power descriptor in the EEPROM should be programmed to match the current draw of the device.

A Ferrite Bead is connected in series with USB power to prevent noise from the device and associated circuitry (EMI) being radiated down the USB cable to the Host. The value of the Ferrite Bead depends on the total current required by the circuit – a suitable range of Ferrite Beads is available from Steward (www.steward.com) for example Steward Part # **MI0805K400R-00 also available as DigiKey Part #** 240-1035-1.

Figure 8
USB Self Powered Configuration

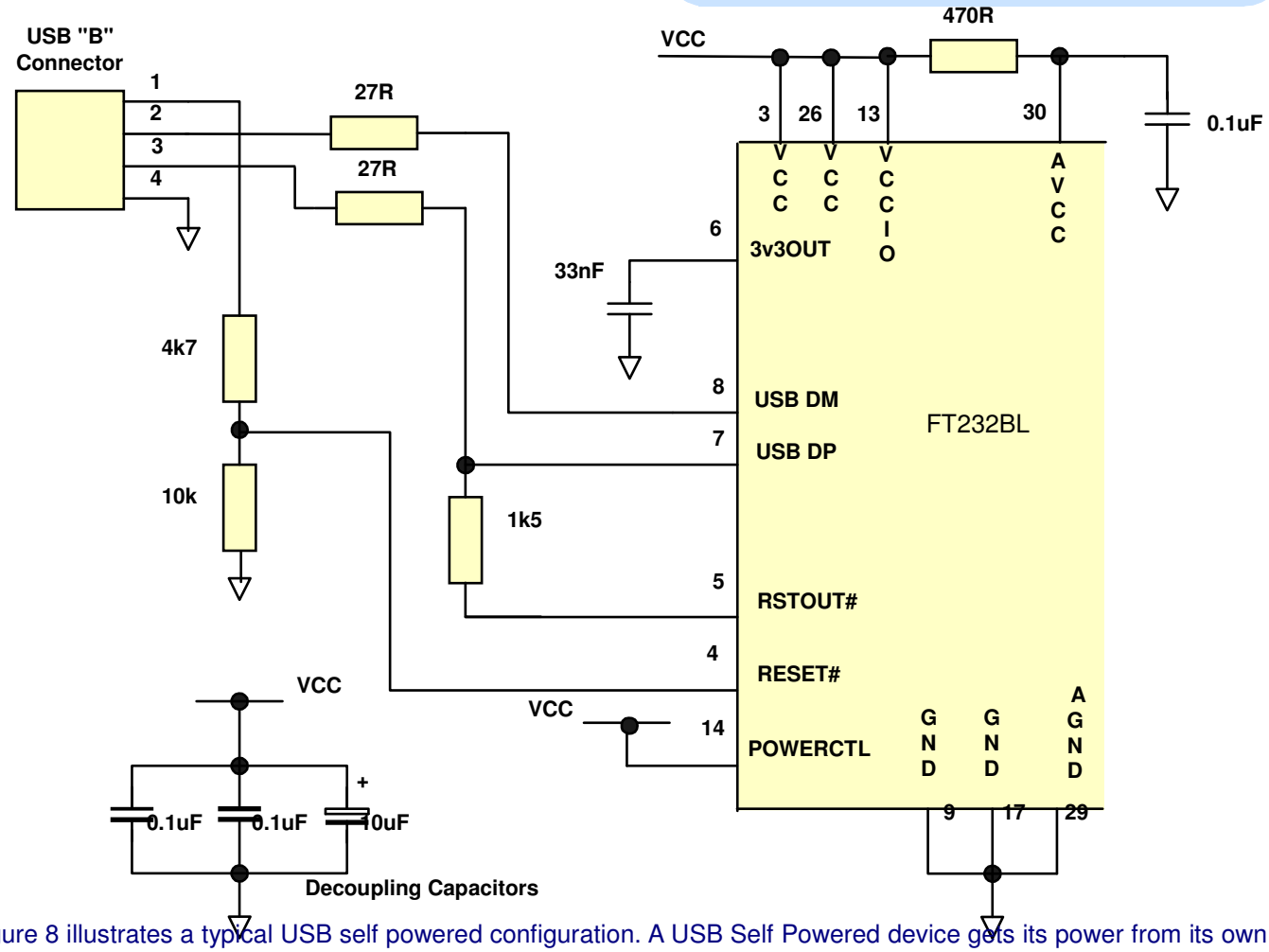


Figure 8 illustrates a typical USB self powered configuration. A USB Self Powered device gets its power from its own POWER SUPPLY and does not draw current from the USB bus. The basic rules for USB Self power devices are as follows –

a) A Self-Powered device should not force current down the USB bus when the USB Host or Hub Controller is powered down.

b) A Self Powered Device can take as much current as it likes during normal operation and USB suspend as it has its own POWER SUPPLY.

c) A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hubs

PWRCTL (pin 14) is pulled high to tell the device to use a USB Bus Power descriptor. The power descriptor in the EEPROM should be programmed to a value of zero. The USB power descriptor option in the EEPROM should be programmed to a value of zero (self powered).

To meet requirement a) the 1.5K pull-up resistor on USBDP is connected to RSTOUT# as per the bus-power circuit. However, the USB Bus Power is used to control the RESET# Pin of the FT232BL device. When the USB Host or Hub is powered up RSTOUT# will pull the 1.5K resistor on USBDP to 3.3V, thus identifying the device as a full speed device to USB. When the USB Host or Hub power is off, RESET# will go low and the device will be held in reset. As RESET# is low, RSTOUT# will also be low, so no current will be forced down USBDP via the 1.5K pull-up resistor when the host or hub is powered down. Failure to do this may cause some USB host or hub controllers to power up erratically.

Note : When the FT232BL is in reset, the UART interface pins all go tri-state. These pins have internal 200K pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

7.4 UART Interface Configuration

Figure 9
USB <=> RS232 Converter Configuration

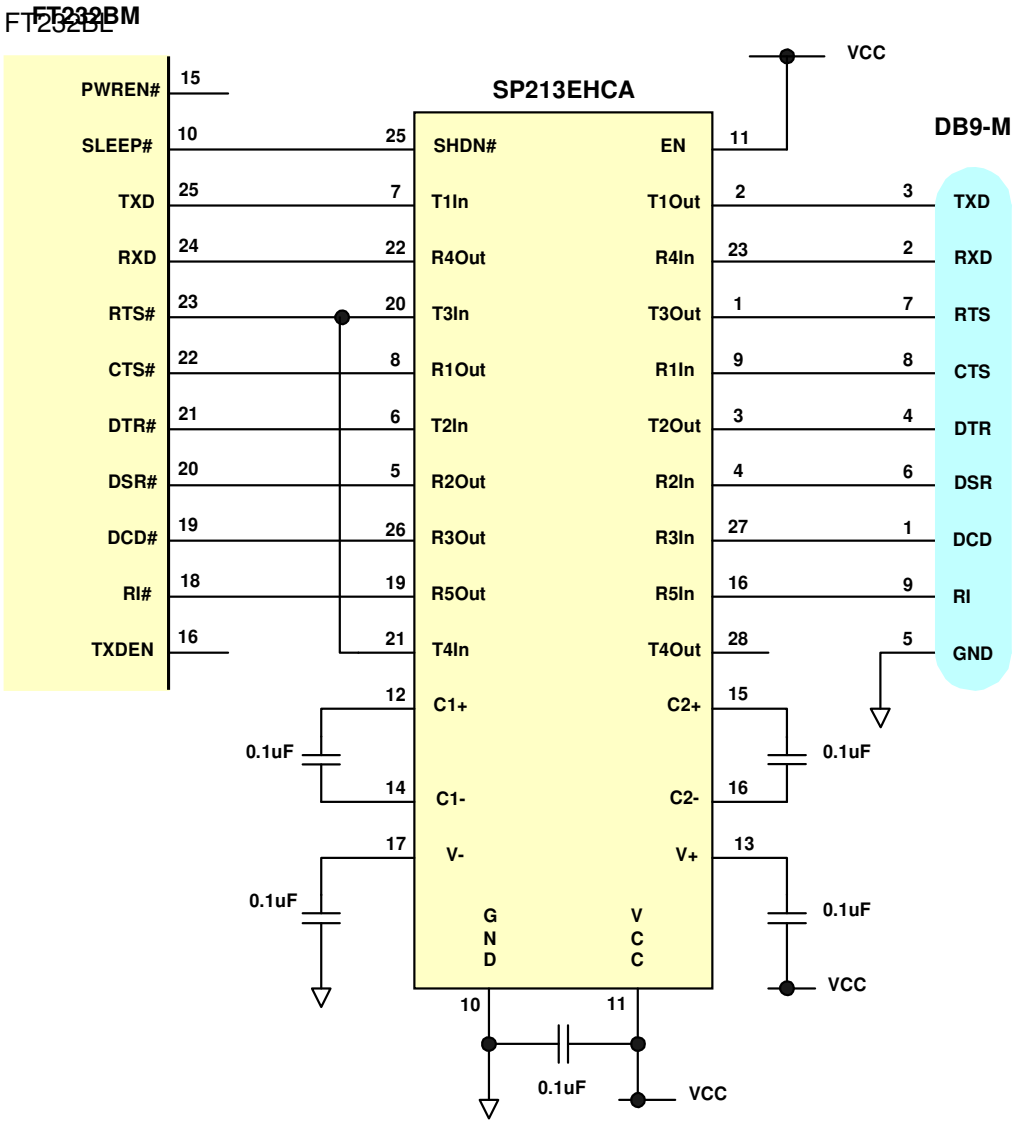


Figure 9 illustrates how to connect the UART interface of the FT232BL to a TTL – RS232 Level Converter I.C. to make a USB <=> RS232 converter using the popular “213” series of TTL to RS232 level converters. These devices have 4 transmitters and 5 receivers in a 28 LD SSOP package and feature an in-built voltage converter to convert the 5v (nominal) VCC to the +/- 9 volts required by RS232. An important feature of these devices is the SHDN# pin which can power down the device to a low quiescent current during USB suspend mode

The device used in the example is a Sipex SP213EHCA which is capable of RS232 communication at up to 500K baud. If a lower baud rate is acceptable, then several pin compatible alternatives are available such as Sipex SP213ECA , Maxim MAX213CAI and Analog Devices ADM213E which are good for communication at up to 115,200 baud. If a higher baud rate is desired, use a Maxim MAX3245CAI part which is capable of RS232 communication at rates of up to 1M baud. The MAX3245 is not pin compatible with the 213 series devices, also its SHDN pin is active high so connect this to PWREN# instead of SLEEP#.

Figure 10
USB <=> RS422 Converter Configuration

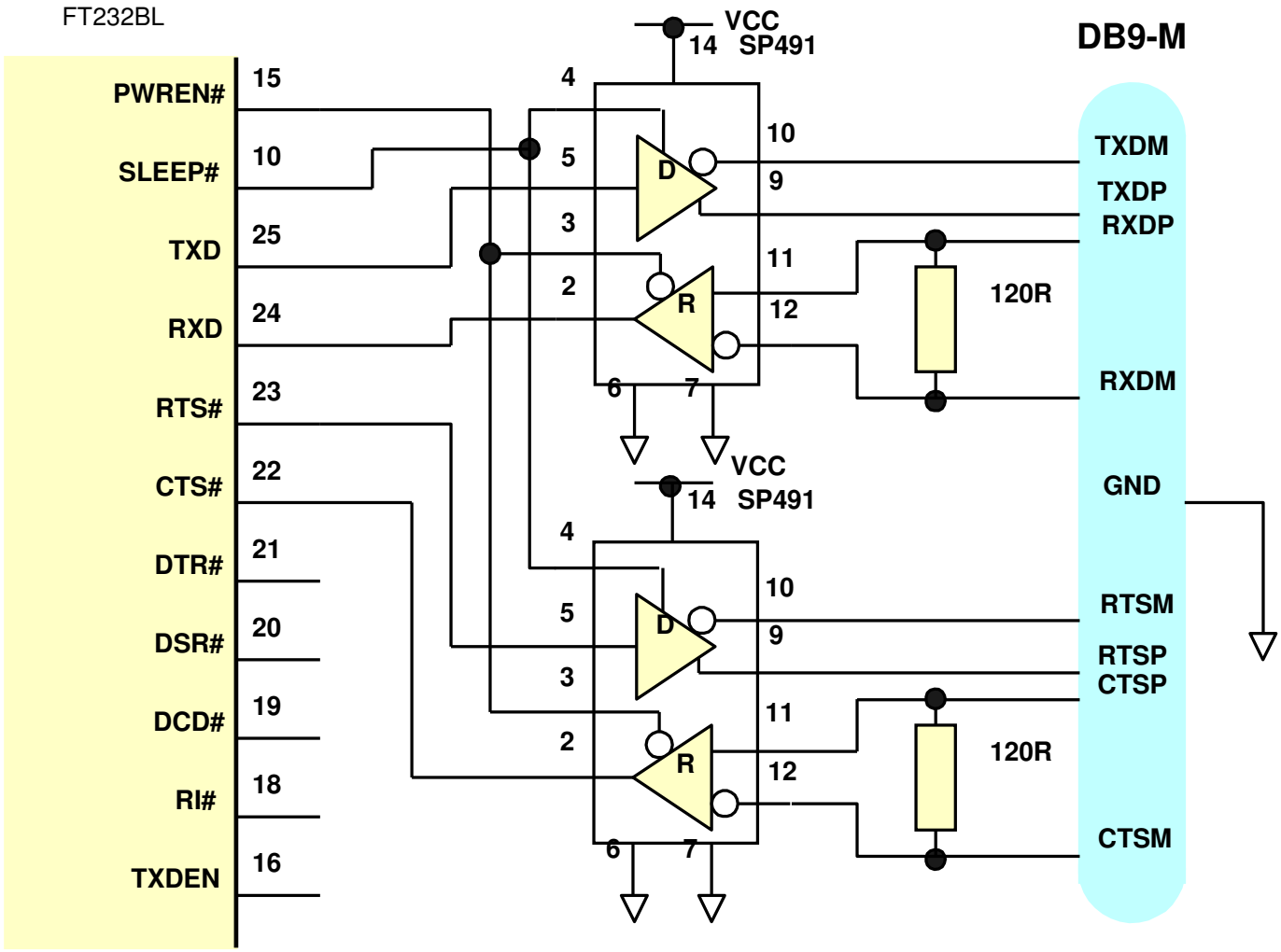


Figure 10 illustrates how to connect the UART interface of the FT232BL to a TTL – RS422 Level Converter I.C. to make a USB <=> RS422 converter. There are many such level converter devices available – this example uses Sipex SP491 devices which have enables on both the transmitter and receiver. Because the transmitter enable is active high, it is connected to the SLEEP# pin. The receiver enable is active low and is connected to the PWREN# pin. This ensures that both the transmitters and receivers are enabled when the device is active, and disabled when the device is in USB suspend mode. If the design is USB BUS powered, it may be necessary to use a P-Channel logic level MOSFET (controlled by PWREN#) in the VCC line of the SP491 devices to ensure that the USB standby current of 500uA is met.
The SP491 is good for sending and receiving data at a rate of up to 5M Baud – in this case the maximum rate is limited to 3M Baud by the FT232BL.

Figure 11
USB <=> RS485 Converter Configuration

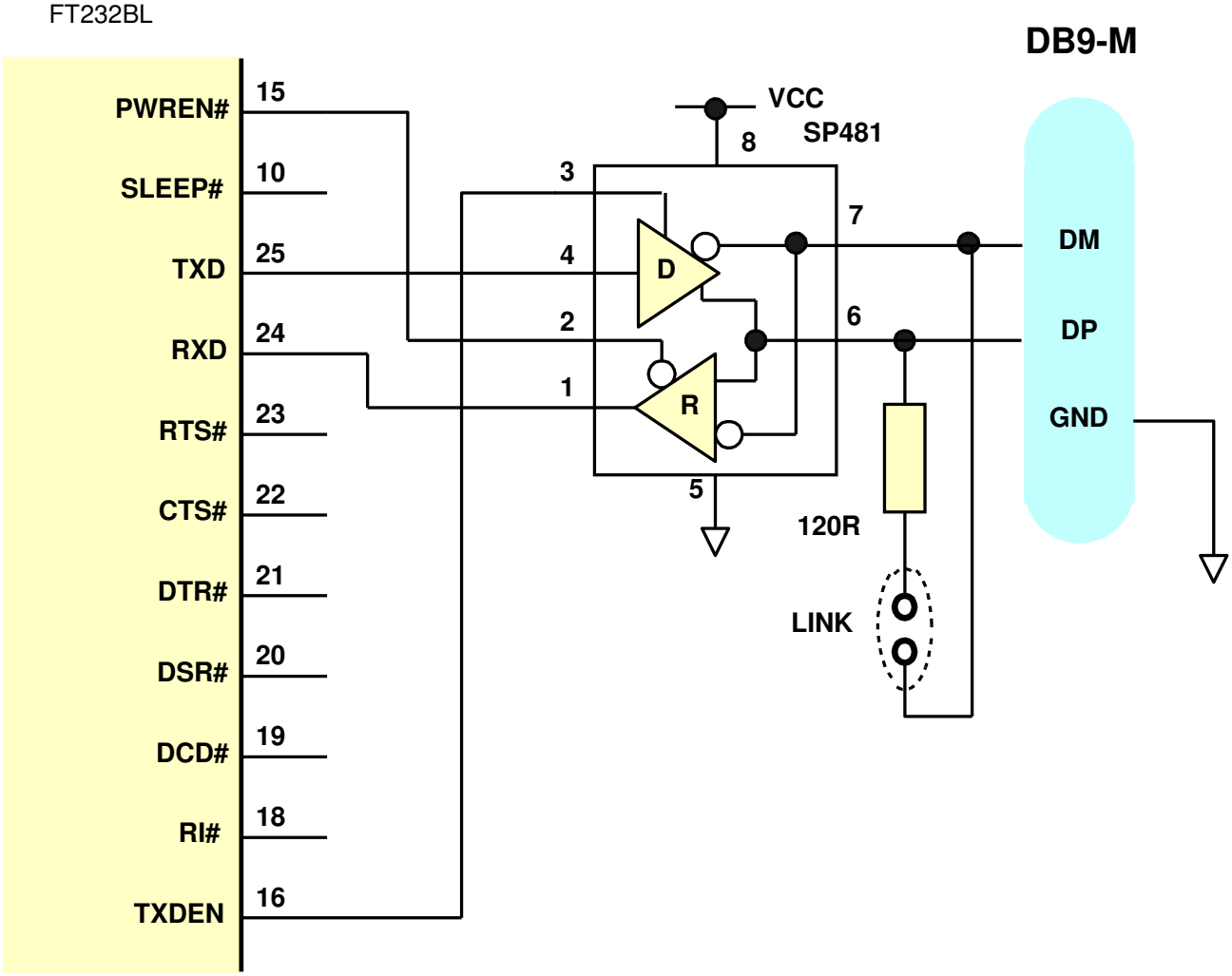


Figure 11 illustrates how to connect the UART interface of the FT232BL to a TTL – RS485 Level Converter I.C. to make a USB => RS485 converter. This example uses the Sipex SP481 device but there are similar parts available from Maxim and Analog Devices amongst others. The SP481 is a RS485 device in a compact 8 pin SOP package. It has separate enables on both the transmitter and receiver. With RS485, the transmitter is only enabled when a character is being transmitted from the UART. The TXDEN pin on the FT232BL is provided for exactly that purpose and so the transmitter enable is wired to TXDEN. The receiver enable is active low, so it is wired to the PWREN# pin to disable the receiver when in USB suspend mode.

RS485 is a multi-drop network – i.e. many devices can communicate with each other over a single two wire cable connection. The RS485 cable requires to be terminated at each end of the cable. A link is provided to allow the cable to be terminated if the device is physically positioned at either end of the cable.

In this example the data transmitted by the FT232BL is also received by the device that is transmitting. This is a common feature of RS485 and requires the application software to remove the transmitted data from the received data stream. With the FT232BL it is possible to do this entirely in hardware – simply modify the schematic so that RXD of the FT232BL is the logical OR of the SP481 receiver output with TXDEN using an HC32 or similar logic gate.

7.5 LED Interface

Figure 12
Dual LED Configuration

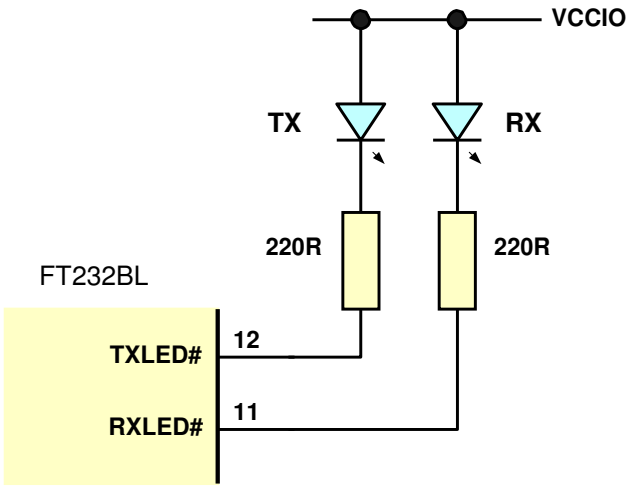
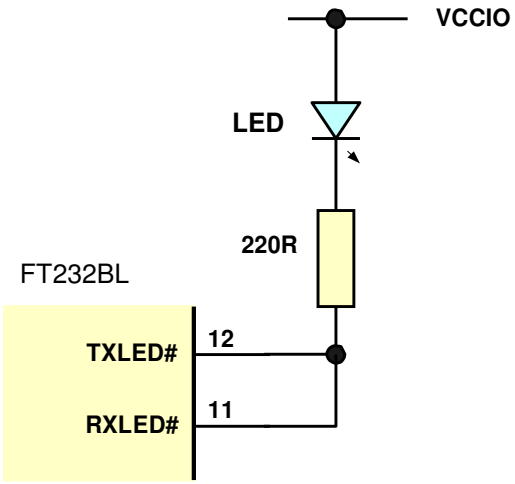


Figure 13
Single LED Configuration



The FT232BL has two IO pins dedicated to controlling LED status indicators, one for transmitted data the other for received data. When data is being transmitted / received the respective pins drive from tri-state to low in order to provide indication on the LEDs of data transfer. A digital one-shot timer is used so that even a small percentage of data transfer is visible to the end user. Figure 12 shows a configuration using two individual LED's – one for transmitted data the other for received data. In Figure 13, the transmit and receive LED indicators are wire-OR'ed together to give a single LED indicator which indicates any transmit or receive data activity.
Another possibility (not shown here) is to use a 3 pin common anode tri-color LED based on the circuit in Figure 13 to have a single LED that can display activity in a variety of colors depending on the ratio of transmit activity compared to receive activity.

Note that the LED's are connected to VCCIO.

 © Future Technology Devices Intl. Ltd. 2005

7.6 Interfacing to 3.3v Logic

Figure 14
Bus Powered Circuit with 3.3V logic drive / supply voltage

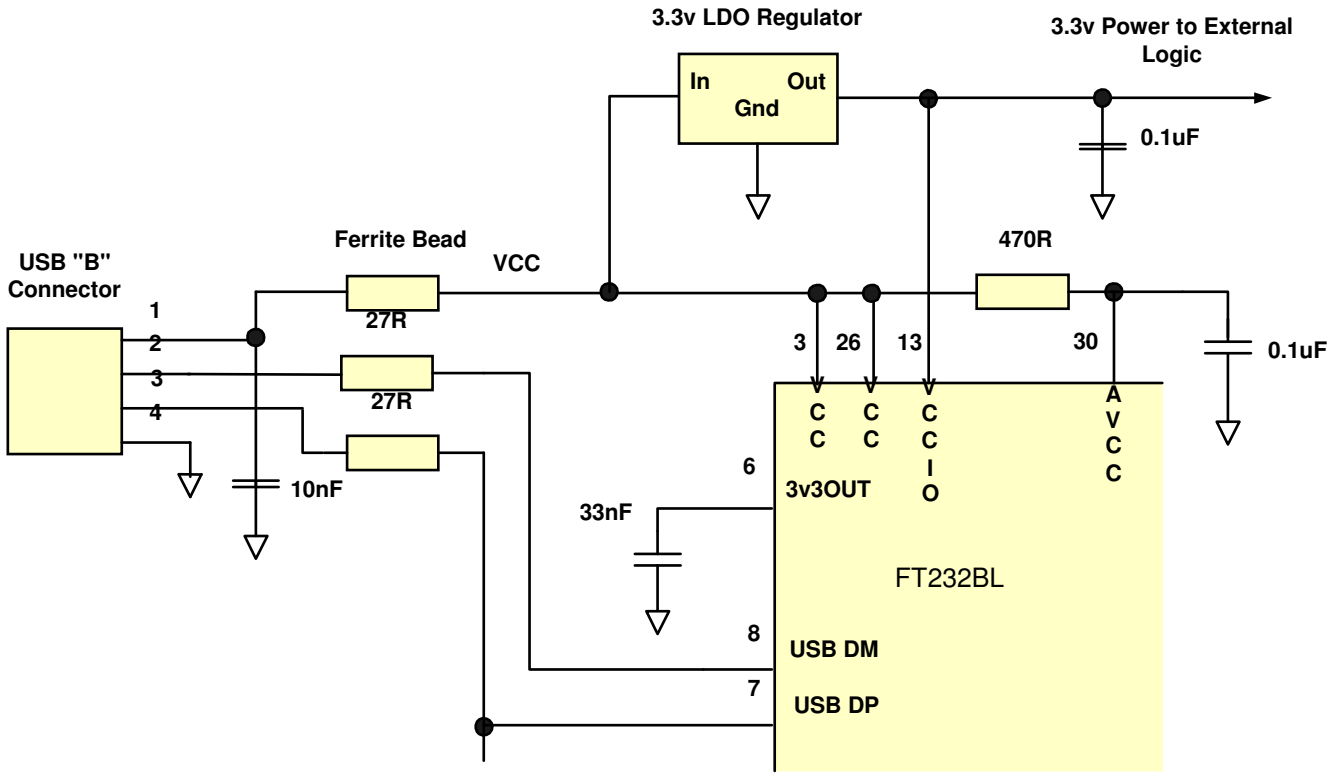


Figure 14 shows how to configure the FT232BL to interface with a 3.3V logic device. In this example, a discrete 3.3V regulator is used to supply the 3.3V logic from the USB supply. VCCIO is connected to the output of the 3.3V regulator, which in turn will cause the UART interface IO pins to drive out at 3.3V level. For USB bus powered circuits some considerations have to be taken into account when selecting the regulator –

a) The regulator must be capable of sustaining its output voltage with an input voltage of 4.35 volts. A Low Drop Out (LDO) regulator must be selected.
b) The quiescent current of the regulator must be low in order to meet the USB suspend total current requirement of <= 500uA during USB suspend.

An example of a regulator family that meets these requirements is the MicroChip (Telcom) TC55 Series. These devices can supply up to 250mA current and have a quiescent current of under 1uA.

In some cases, where only a small amount of current is required (< 5mA) , it may be possible to use the in-built regulator of the FT232BL to supply the 3.3v without any other components being required. In this case, connect VCCIO to the 3v3OUT pin of the FT232BL.

Note : It should be emphasised that the 3.3V supply for VCCIO in a bus powered design with a 3.3V logic interface should come from an LDO which is supplied by the USB bus, or from the 3V3OUT pin of the FT232BL, and not from any other source.

Figure 15
Self Powered Circuit with 3.3V logic drive / supply voltage

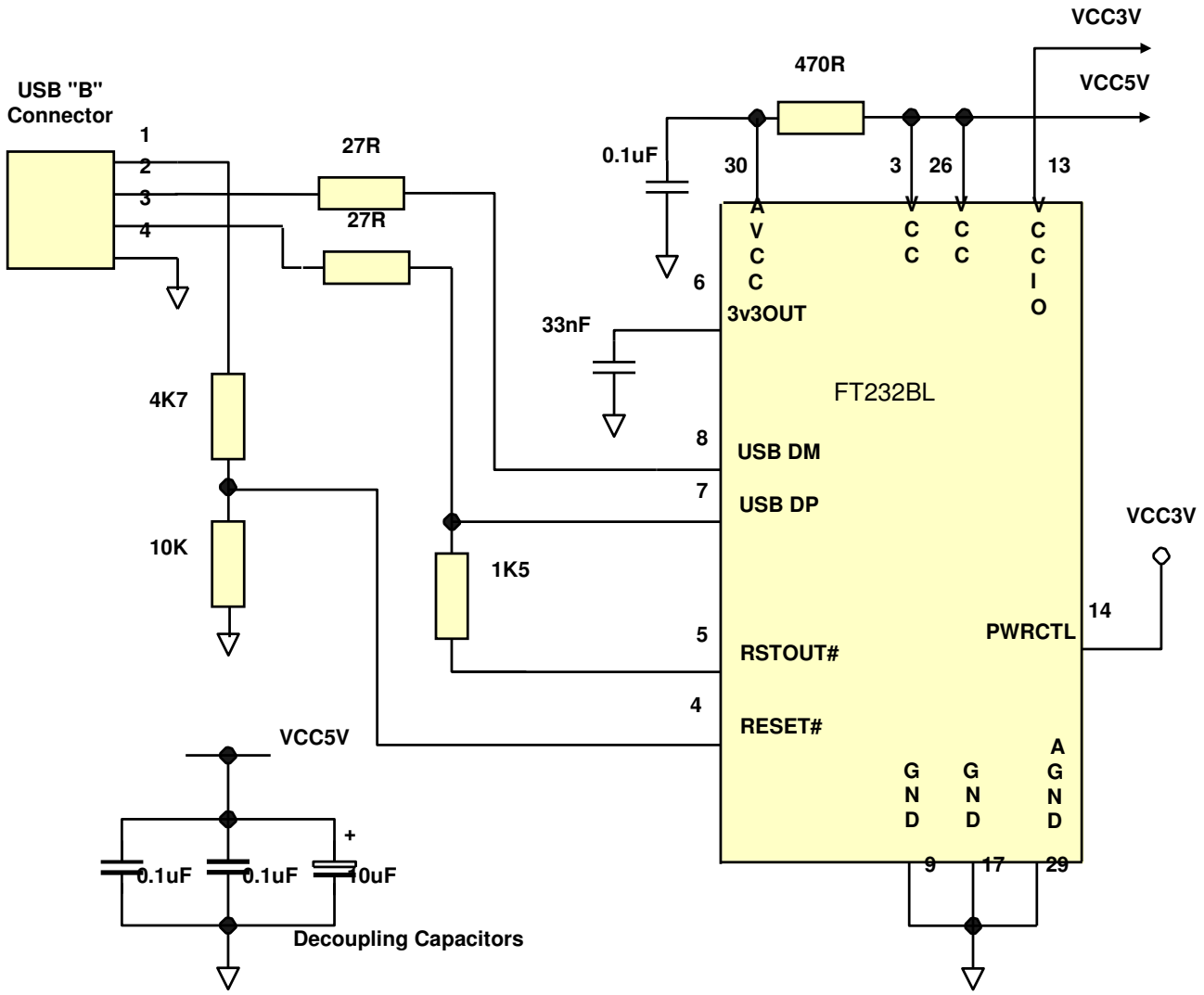


Figure 15 is an example of a USB self powered design with 3.3V interface. In this case VCCIO is supplied by an external 3.3V supply in order to make the device IO pins drive out at 3.3V logic level, thus allowing it to be connected to a 3.3V MCU or other external logic. A USB self powered design uses its own power supplies, and does not draw any of its power from the USB bus. In such cases, no special care need be taken to meet the USB suspend current (0.5 mA) as the device does not get its power from the USB port.

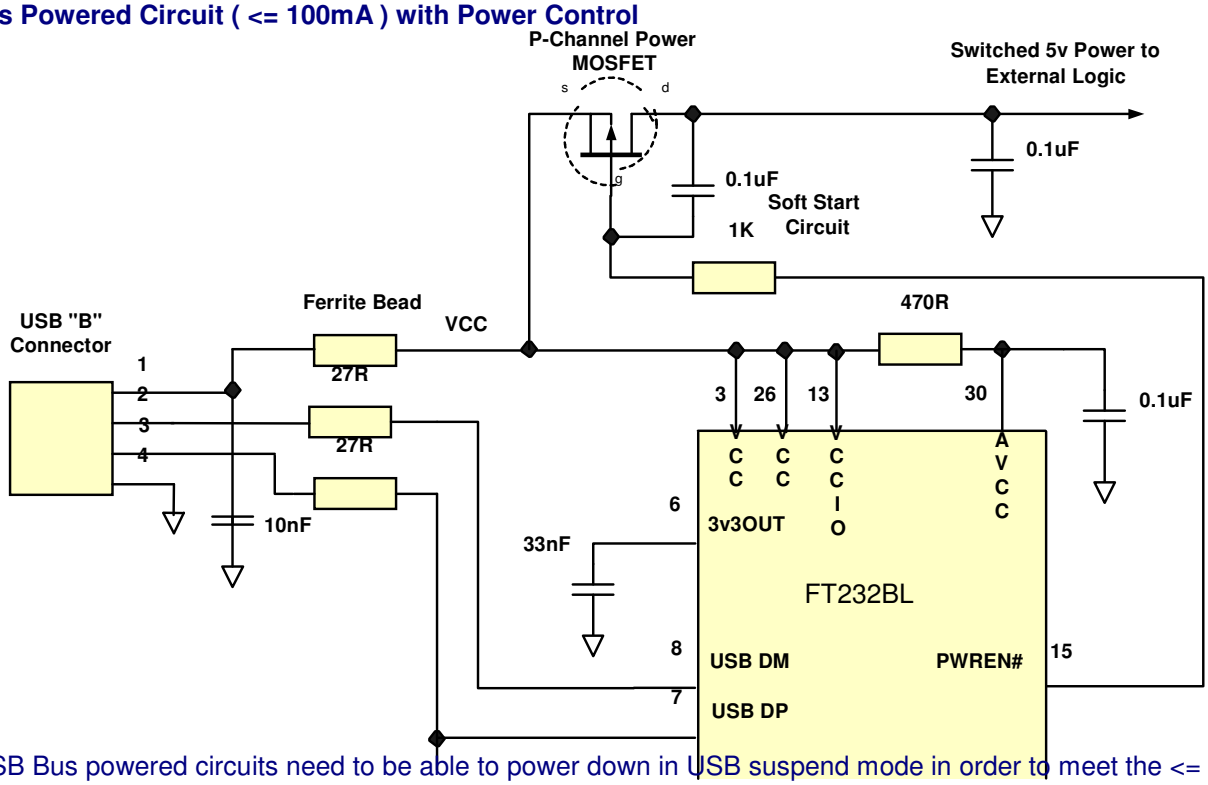
As with bus powered 3.3V interface designs, in some cases, where only a small amount of current is required (<5mA), it may be possible to use the in-built regulator of the FT232BL to supply the 3.3V without any other components being required. In this case, connect VCCIO to the 3v3OUT pin of the FT232BL.

Note that in this case PWRCTL is pulled up to VCCIO, not VCC.

7.7 Power Switching

Figure 16

Bus Powered Circuit (<= 100mA) with Power Control



USB Bus powered circuits need to be able to power down in USB suspend mode in order to meet the <= 500uA total suspend current requirement (including external logic). Some external logic can power itself down into a low current state by monitoring the PWREN# pin. For external logic that cannot power itself down in that way, the FT232BL provides a simple but effective way of turning off power to external circuitry during USB suspend.

Figure 16 shows how to use a discrete P-Channel Logic Level MOSFET to control the power to external logic circuits. A suitable device could be a Fairchild NDT456P, or International Rectifier IRLML6402, or equivalent. It is recommended that a “soft start” circuit consisting of a 1K series resistor and a 0.1 uF capacitor are used to limit the current surge when the MOSFET turns on. Without the soft start circuit there is a danger that the transient power surge of the MOSFET turning on will reset the FT232BL, or the USB host / hub controller. The values used here allow attached circuitry to power up with a slew rate of ~12.5 V per millisecond, in other words the output voltage will transition from GND to 5V in approximately 400 microseconds.

Alternatively, a dedicated power switch i.c. with inbuilt “soft-start” can be used instead of a MOSFET. A suitable power switch I.C. for such an application would be a Micrel (www.micrel.com) MIC2025-2BL or equivalent.

Please note the following points in connection with power controlled designs –

a) The logic to be controlled must have its own reset circuitry so that it will automatically reset itself when power is re-applied on coming out of suspend.

b) Set the Pull-down on Suspend option in the FT232BL’s EEPROM.

c) For USB high-power bus powered device (one that consumes greater than 100 mA, and up to 500 mA of current from the USB bus), the power consumption of the device should be set in the max power field in the EEPROM. A high-power bus powered device must use this descriptor in the EEPROM to inform the system of its power requirements.

d) For 3.3V power controlled circuits VCCIO must not be powered down with the external circuitry (PWREN# gets its VCC supply from VCCIO). Either connect the power switch between the output of the 3.3V regulator and the external 3.3V logic OR if appropriate power VCCIO from the 3V3OUT pin of the FT232BL.

8.0 Document Revision History

DS232B Version 1.0 – Initial document created 30 April 2002.

DS232B Version 1.1 – Updated 04 August 2002

Section 4.1 RESET# Pin description corrected (RESET# does not have an internal 200k pull-up to VCC as previously stated).
Figure 2 pin-out corrected (EECS = Pin 32).

DS232B Version 1.2 – Updated 27 October 2003

Pin and package naming made consistent throughout data sheet.
Section 1.0 Updated to reflect availability of Mac OS X driver.
Section 2.0 Minor corrections.
Section 3.1 Minor changes to functional block descriptions of SIE, RESET Generator, and EEPROM interface.
Section 4.1 Note added to EEPROM interface group.
Section 4.1 RSTOUT# Pin description amended.
Section 6.1 Minimum operating supply voltage adjusted.
Section 6.1 EESK added to Note 3.
Section 6.1 UART IO pin characteristics amended.
Section 6.1 RESET#, TEST, EECS, EESK, and EEDATA pin characteristics amended.
Section 6.1 RSTOUT pin characteristics amended.
Section 7.1 Updated recommended ceramic resonator part number and circuit configuration.
Section 7.3 “USB Self Powered Configuration (1)” (original figure 8 removed). Recommended circuit for USB self powered designs updated. Subsequent figure numbers have changed as a result.
Section 7.6 Note added to description of Bus powered circuit with 3.3V logic drive / supply voltage.
Section 7.6 Self Powered Circuit with 3.3V logic drive / supply voltage added (new figure 16).

DS232B Version 1.3 – Updated 10 December 2003

Section 5.0 Package drawing amended
Section 6.0 Floor Life / Relative Humidity specification added. ESD and Latch Up specifications amended.
Section 7.1 Required resonator / crystal accuracy corrected.

DS232B Version 1.4 – Updated 10 February 2004

Grammar Correcttions
Section 10.0 FTDI Address Updated
Section 2.0 Extended EEPROM Support corrected
Section 4.1 VCCIO Pin description amended.
Section 7.4 RS485 Example Sipex SP481 part number corrected.

DS232B Version 1.5 – Updated April 2004

Section 4.1 EESK Pin Description amended.
Section 7.6 Figure 16 PWRCTL Pin number corrected.
Section 7.7 Figure 15 PWREN# Pin number corrected.

DS232B Version 1.6 – Updated November 2004

Section 1.0 WinCE drivers now available.
Section 5.0 Date code format updated.
Section 6.0 Absolute Maximum Ratings table reformated.

DS232B Version 1.7 – Updated February 2005

Section 1.0 D2XX drivers for Linux and Windows CE now available.
Section 5.0 FT232BL (lead Free) and FT232BQ (lead free QFN package) now available.

DS232B Version 1.8 – Updated December 2005

Section 1.0 Driver OS Support updated.
Section 6.0 USB Data line absolute maximum rating added.

BC847/BC547 series

45 V, 100 mA NPN general-purpose transistors

Rev. 06 — 19 May 2005 Product data sheet

1. Product profile

1.1 General description

NPN general-purpose transistors.

Table 1: Product overview

Type number [1]	Package		PNP complement
	Philips	JEITA	
BC847	SOT23	-	BC857
BC847W	SOT323	SC-70	BC857W
BC847T	SOT416	SC-75	BC857T
BC847AM	SOT883	SC-101	BC857AM
BC847BM	SOT883	SC-101	BC857BM
BC847CM	SOT883	SC-101	BC857CM
BC547 [2]	SOT54	SC-43A	BC557

[1] Valid for all available selection groups.

[2] Also available in SOT54A and SOT54 variant packages (see Section 2).

1.2 Features

- Low current
- Low voltage
- Three different gain selections

1.3 Applications

- General-purpose switching and amplification

1.4 Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	45	V
I_C	collector current (DC)		-	-	100	mA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 2 mA				
	h_{FE} group A		110	180	220	
	h_{FE} group B		200	290	450	
	h_{FE} group C		420	520	800	

9.0 Disclaimer

© Future Technology Devices International Limited, 2005

Neither the whole nor any part of the information contained in, or the product described in this manual, may be adapted or reproduced in any material or electronic form without the prior written consent of the copyright holder. This product and its documentation are supplied on an as-is basis and no warranty as to their suitability for any particular purpose is either made or implied.

Future Technology Devices International Ltd. will not accept any claim for damages howsoever arising as a result of use or failure of this product. Your statutory rights are not affected.

This product or any variant of it is not intended for use in any medical appliance, device or system in which the failure of the product might reasonably be expected to result in personal injury.

This document provides preliminary information that may be subject to change without notice.

10.0 Contact Information

Head Office -

Future Technology Devices International Ltd.
373 Scotland Street,
Glasgow G5 8QB,
United Kingdom

Tel. : +(44) 141 429 2777
Fax. : +(44) 141 429 2758

E-Mail (Sales) : sales1@ftdichip.com
E-Mail (Support) : support1@ftdichip.com
E-Mail (General Enquiries) : admin1@ftdichip.com

Regional Sales Offices -

Future Technology Devices International Ltd. (Taiwan)
4F, No 16-1,
Sec. 6 Mincyuan East Road,
Neihu District,
Taipei 114,
Taiwan, R.o.C.

Tel.: +886 2 8791 3570
Fax: +886 2 8791 3576

E-Mail (Sales): tw.sales@ftdichip.com
E-Mail (Support): tw.support@ftdichip.com
E-Mail (General Enquiries): tw.admin@ftdichip.com

Website URL : http://www.ftdichip.com

Future Technology Devices International Ltd. (USA)
5285 NE Elam Young
Parkway, Suite B800
Hillsboro,
OR 97124-6499
USA

Tel.: +1 (503) 547-0988
Fax: +1 (503) 547-0987

E-Mail (Sales): us.sales@ftdichip.com
E-Mail (Support): us.support@ftdichip.com
E-Mail (General Enquiries): us.admin@ftdichip.com

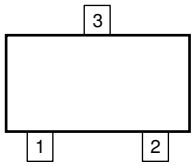
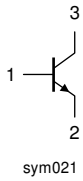
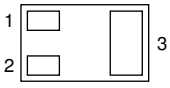
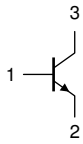
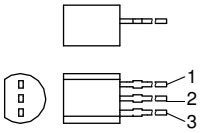
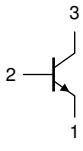
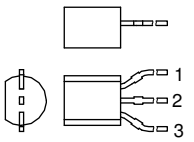
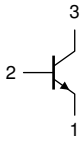
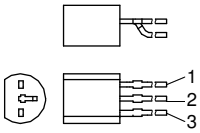
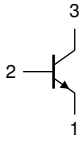
Agents and Sales Representatives

At the time of writing our Sales Network covers over 40 different countries world-wide. Please visit the Sales Network page of our Web site for the contact details our distributor(s) in your country.

PHILIPS

2. Pinning information

Table 3: Pinning

Pin	Description	Simplified outline	Symbol
SOT23, SOT323, SOT416			
1	base	 006aaa144	 sym021
2	emitter		
3	collector		
SOT883			
1	base	 Transparent top view	 sym021
2	emitter		
3	collector		
SOT54			
1	emitter	 001aab347	 sym026
2	base		
3	collector		
SOT54A			
1	emitter	 001aab348	 sym026
2	base		
3	collector		
SOT54 variant			
1	emitter	 001aab447	 sym026
2	base		
3	collector		

© Koninklijke Philips Electronics N.V. 2005. All rights reserved.

3. Ordering information

Table 4: Ordering information

Type number [1]	Package		
	Name	Description	Version
BC847	-	plastic surface mounted package; 3 leads	SOT23
BC847W	SC-70	plastic surface mounted package; 3 leads	SOT323
BC847T	SC-75	plastic surface mounted package; 3 leads	SOT416
BC847AM	SC-101	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
BC847BM			
BC847CM			
BC547 [2]	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54

[1] Valid for all available selection groups.

[2] Also available in SOT54 and SOT54 variant packages (see Section 2 and Section 9).

4. Marking

Table 5: Marking codes

Type number	Marking code [1]	Type number	Marking code [1]
BC847	1H*	BC847AT	1E
BC847A	1E*	BC847BT	1F
BC847B	1F*	BC847CT	1G
BC847C	1G*	BC847AM	D4
BC847W	1H*	BC847BM	D5
BC847AW	1E*	BC847CM	D6
BC847BW	1F*	BC547	C547
BC847CW	1G*	BC547B	C547B
BC847T	1N	BC547C	C547C

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

© Koninklijke Philips Electronics N.V. 2005. All rights reserved.

5. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	45	V
V_{EBO}	emitter-base voltage	open collector		-	6	V
I_C	collector current (DC)			-	100	mA
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	200	mA
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms		-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	SOT23		[1]	-	250	mW
	SOT323		[1]	-	200	mW
	SOT416		[1]	-	150	mW
	SOT883		[2] [3]	-	250	mW
	SOT54		[1]	-	500	mW
T_{stg}	storage temperature			−65	+150	°C
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			−65	+150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

[3] Device mounted on an FR4 PCB with 60 µm copper strip line, standard footprint.

6. Thermal characteristics

Table 7: Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air					
	SOT23		[1]	-	-	500	K/W
	SOT323		[1]	-	-	625	K/W
	SOT416		[1]	-	-	833	K/W
	SOT883		[2] [3]	-	-	500	K/W
	SOT54		[1]	-	-	250	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

[3] Device mounted on an FR4 PCB with 60 µm copper strip line, standard footprint.

© Koninklijke Philips Electronics N.V. 2005. All rights reserved.

7. Characteristics

Table 8: Characteristics

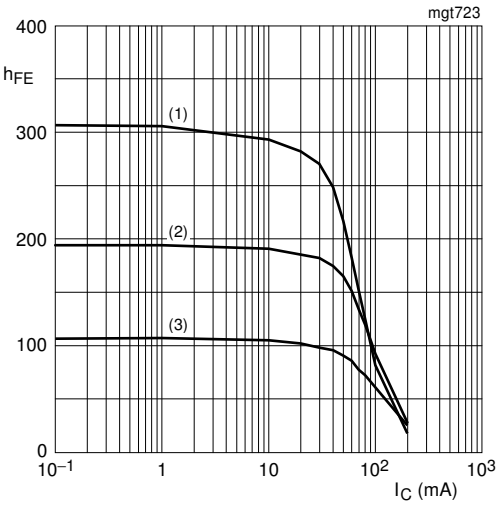
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CBO}	collector-base cut-off current	V_{CB} = 30 V; I_E = 0 A		-	-	15	nA
		V_{CB} = 30 V; I_E = 0 A; T_j = 150 °C		-	-	5	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_E = 0 A		-	-	100	nA
h_{FE}	DC current gain						
	h_{FE} group A	V_{CE} = 5 V; I_C = 10 µA		-	90	-	
	h_{FE} group B	V_{CE} = 5 V; I_C = 10 µA		-	150	-	
	h_{FE} group C	V_{CE} = 5 V; I_C = 10 µA		-	270	-	
	DC current gain	V_{CE} = 5 V; I_C = 2 mA		110	-	800	
	h_{FE} group A	V_{CE} = 5 V; I_C = 2 mA		110	180	220	
	h_{FE} group B	V_{CE} = 5 V; I_C = 2 mA		200	290	450	
	h_{FE} group C	V_{CE} = 5 V; I_C = 2 mA		420	520	800	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA		-	90	200	mV
		I_C = 100 mA; I_B = 5 mA	[1]	-	200	400	mV
V_{BEsat}	base-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA	[2]	-	700	-	mV
		I_C = 100 mA; I_B = 5 mA	[2]	-	900	-	mV
V_{BE}	base-emitter voltage	I_C = 2 mA; V_{CE} = 5 V	[2]	580	660	700	mV
		I_C = 10 mA; V_{CE} = 5 V		-	-	770	mV
C_c	collector capacitance	$I_E = i_e$ = 0 A; V_{CB} = 10 V; f = 1 MHz		-	-	1.5	pF
C_e	emitter capacitance	$I_C = i_c$ = 0 A; V_{EB} = 0.5 V; f = 1 MHz		-	11	-	pF
f_T	transition frequency	I_C = 10 mA; V_{CE} = 5 V; f = 100 MHz		100	-	-	MHz
F	noise figure	I_C = 200 µA; V_{CE} = 5 V; R_S = 2 kΩ; f = 1 kHz; B = 200 Hz		-	2	10	dB

[1] Pulse test: $t_p \leq 300$ µs; $\delta \leq 0.02$.

[2] V_{BE} decreases by approximately 2 mV/K with increasing temperature.

© Koninklijke Philips Electronics N.V. 2005. All rights reserved.



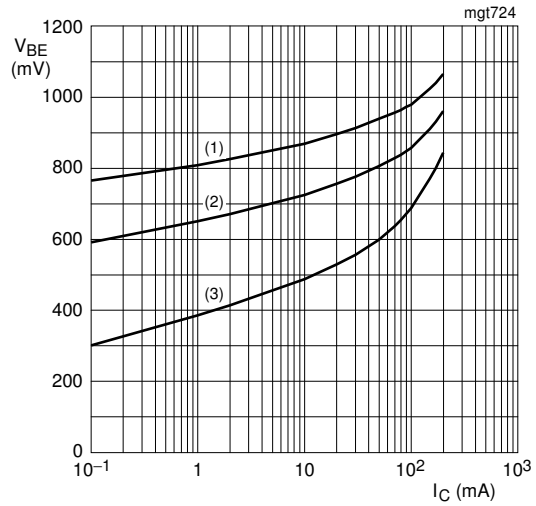
V_{CE} = 5 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 1. Selection A: DC current gain as a function of collector current; typical values



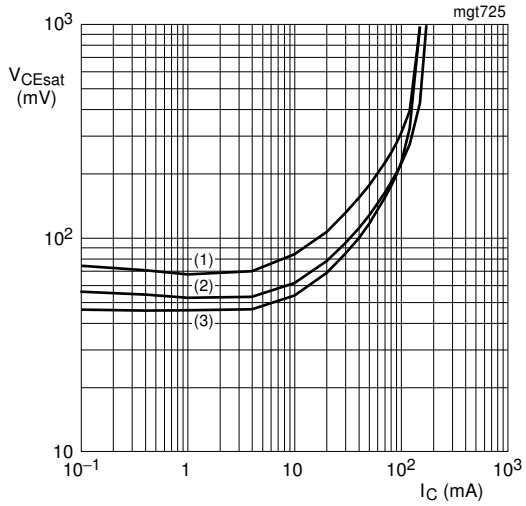
V_{CE} = 5 V

(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 150 °C

Fig 2. Selection A: Base-emitter voltage as a function of collector current; typical values



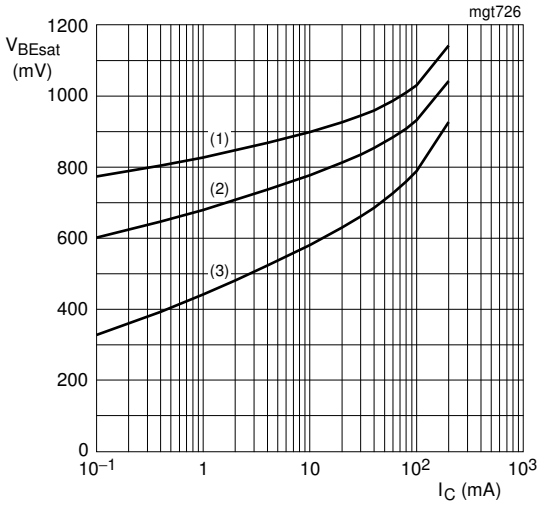
I_C/I_B = 20

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 3. Selection A: Collector-emitter saturation voltage as a function of collector current; typical values



I_C/I_B = 10

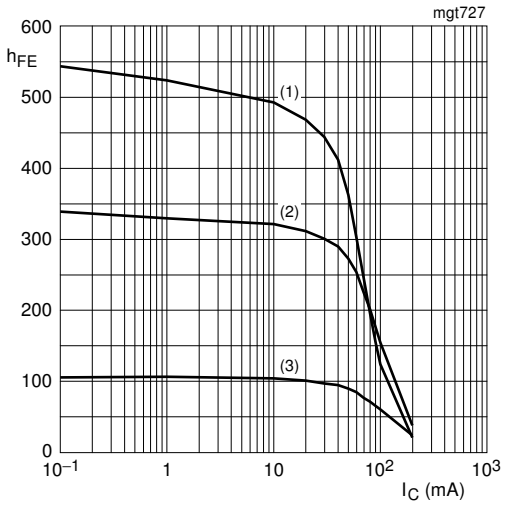
(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 150 °C

Fig 4. Selection A: Base-emitter saturation voltage as a function of collector current; typical values

© Koninklijke Philips Electronics N.V. 2005. All rights reserved.



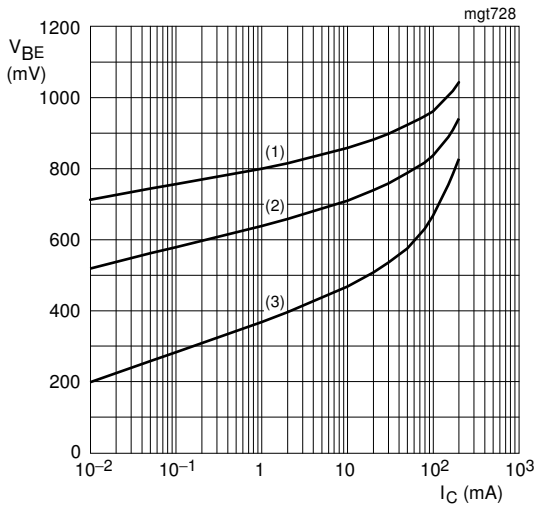
V_{CE} = 5 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 5. Selection B: DC current gain as a function of collector current; typical values



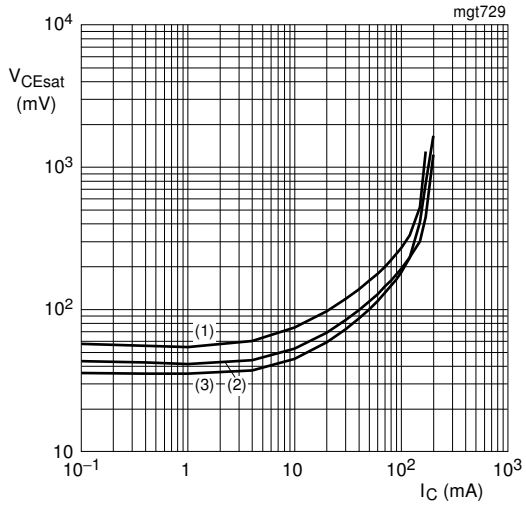
V_{CE} = 5 V

(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 150 °C

Fig 6. Selection B: Base-emitter voltage as a function of collector current; typical values



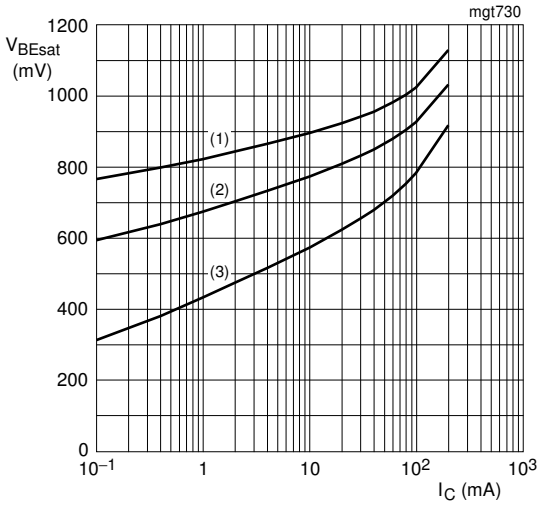
I_C/I_B = 20

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 7. Selection B: Collector-emitter saturation voltage as a function of collector current; typical values



I_C/I_B = 10

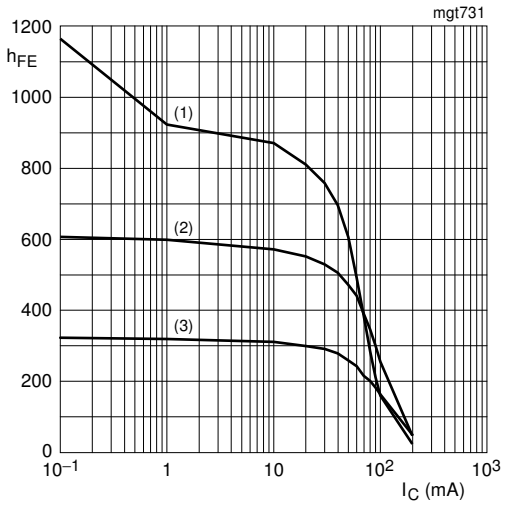
(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 150 °C

Fig 8. Selection B: Base-emitter saturation voltage as a function of collector current; typical values

© Koninklijke Philips Electronics N.V. 2005. All rights reserved.



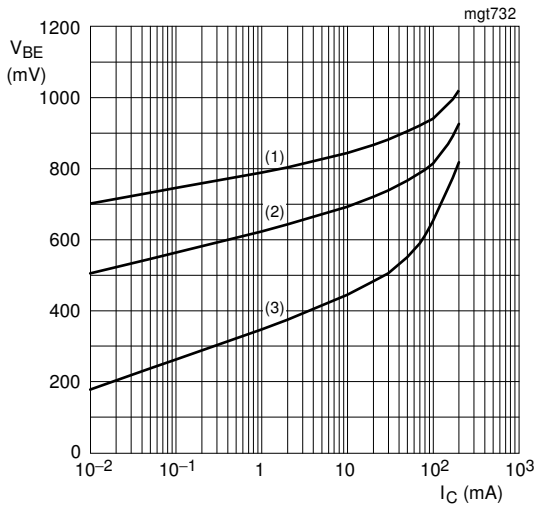
V_{CE} = 5 V

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 9. Selection C: DC current gain as a function of collector current; typical values



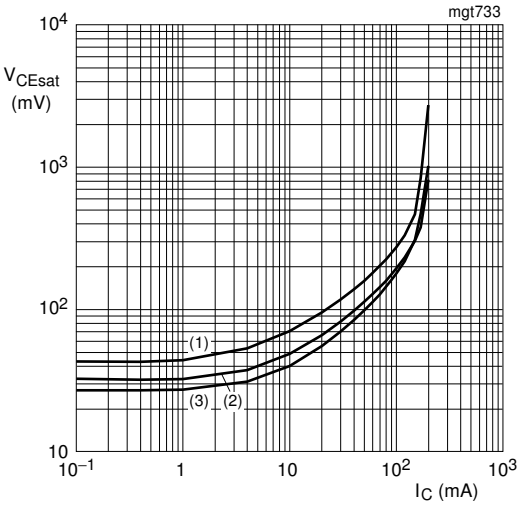
V_{CE} = 5 V

(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 150 °C

Fig 10. Selection C: Base-emitter voltage as a function of collector current; typical values



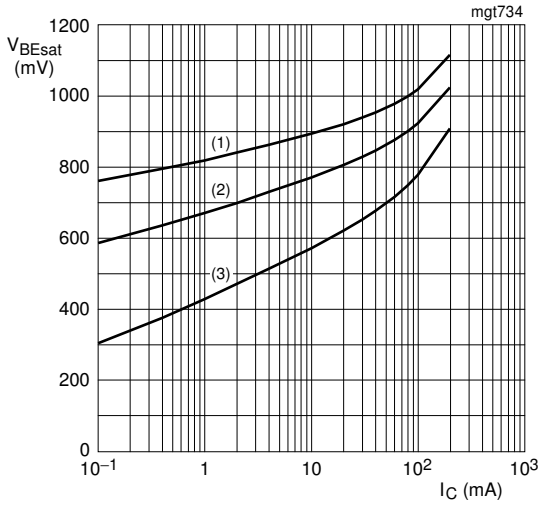
I_C/I_B = 20

(1) T_{amb} = 150 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 11. Selection C: Collector-emitter saturation voltage as a function of collector current; typical values



I_C/I_B = 10

(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 150 °C

Fig 12. Selection C: Base-emitter saturation voltage as a function of collector current; typical values

© Koninklijke Philips Electronics N.V. 2005. All rights reserved.

8. Package outline

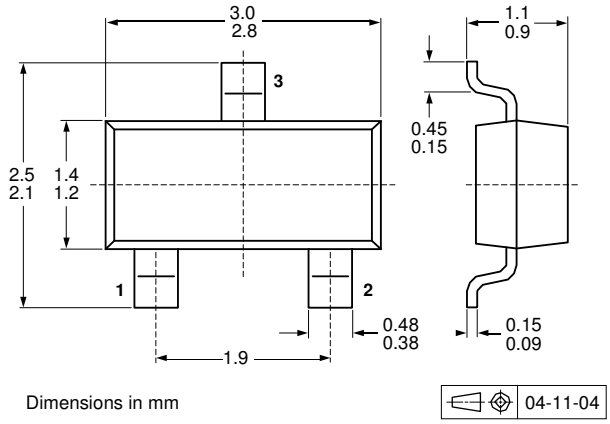


Fig 13. Package outline SOT23 (TO-236AB)

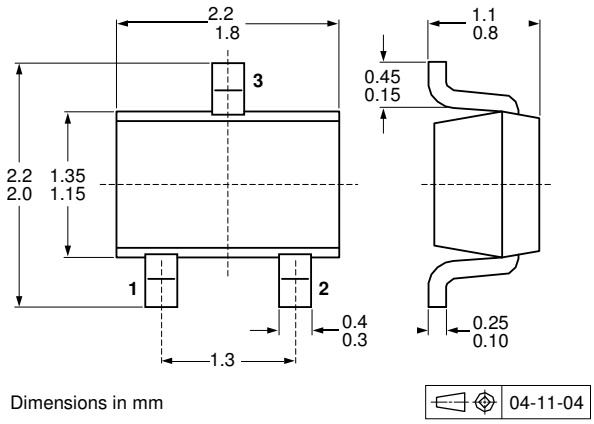


Fig 14. Package outline SOT323 (SC-70)

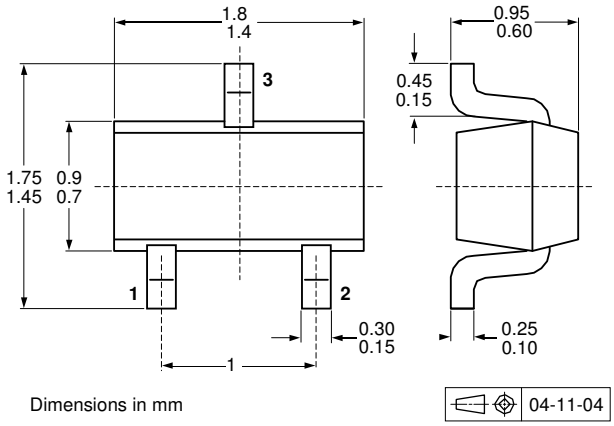


Fig 15. Package outline SOT416 (SC-75)

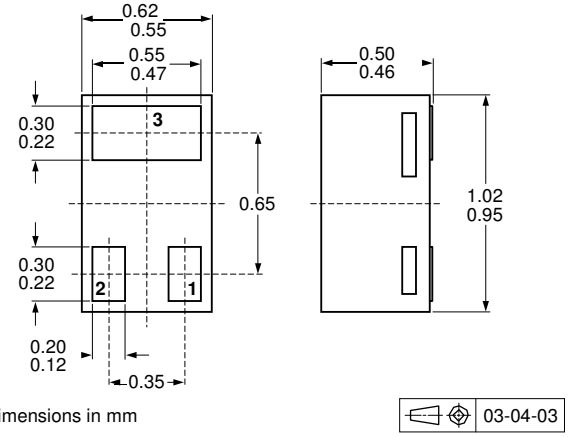


Fig 16. Package outline SOT883 (SC-101)

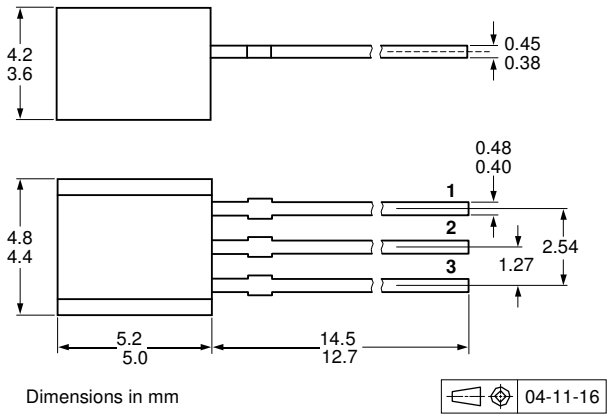


Fig 17. Package outline SOT54 (SC-43A/TO-92)

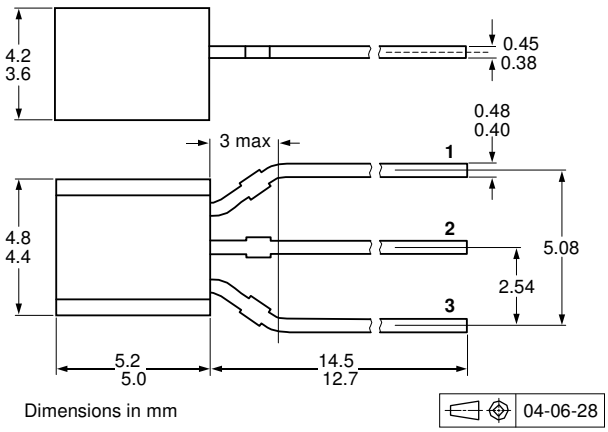


Fig 18. Package outline SOT54A

© Koninklijke Philips Electronics N.V. 2005. All rights reserved.

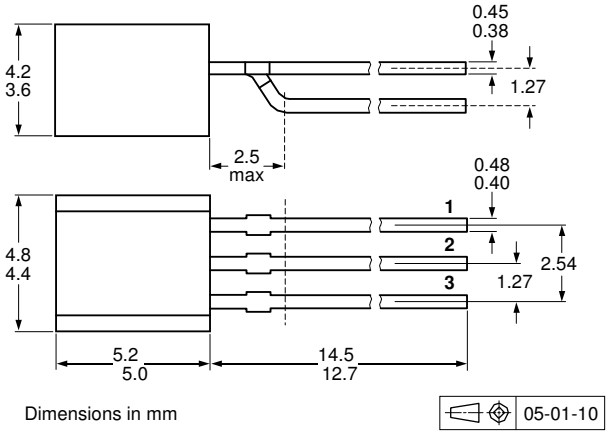


Fig 19. Package outline SOT54 variant

9. Packing information

Table 9: Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code. [1]

Type number [2]	Package	Description	Packing quantity		
			3000	5000	10000
BC847	SOT23	4 mm pitch, 8 mm tape and reel	-215	-	-235
BC847W	SOT323	4 mm pitch, 8 mm tape and reel	-115	-	-135
BC847T	SOT416	4 mm pitch, 8 mm tape and reel	-115	-	-135
BC847AM	SOT883	2 mm pitch, 8 mm tape and reel	-	-	-315
BC847BM					
BC847CM					
BC547	SOT54	bulk, straight leads	-	-412	-
	SOT54A	tape and reel, wide pitch	-	-	-116
		tape ammopack, wide pitch	-	-	-126
	SOT54 variant	bulk, delta pinning	-	-112	-

[1] For further information and the availability of packing methods, see Section 15.

[2] Valid for all available selection groups.

© Koninklijke Philips Electronics N.V. 2005. All rights reserved.

10. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BC847_BC547_SER_6	20050519	Product data sheet	-	9397 750 14609	BC846_BC847_ BC848_5, BC847M_SERIES_2, BC846T_847T_ SERIES_3, BC846W_BC847W_ BC848W_4, BC546_547_4
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • This data sheet is a type combination out of the previous data sheets BC846_BC847_BC848_5, BC847M_SERIES_2, BC846T_847T_SERIES_3, BC846W_BC847W_BC848W_4 and BC546_547_4.				
BC846_BC847_BC848_5	20040206	Product specification	-	9397 750 12395	BC846_BC847_ BC848_4
BC847M_SERIES_2	20040310	Product specification	-	9397 750 12838	BC847M_SERIES_1
BC846T_847T_SERIES_3	20001115	Product specification	-	9397 750 07524	BC846T_847T_2
BC846W_BC847W_ BC848W_4	20020204	Product specification	-	9397 750 09166	BC846W_847W_3
BC546_547_4	20041125	Product specification	-	9397 750 13568	BC546_547_3

© Koninklijke Philips Electronics N.V. 2005. All rights reserved.

11. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

13. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

14. Trademarks

Notice — All referenced brands, product names, service names and trademarks are the property of their respective owners.

15. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

© Koninklijke Philips Electronics N.V. 2005. All rights reserved.

45 V, 100 mA NPN general-purpose transistors

Low Power Consumption

Wide Common-Mode and Differential Voltage Ranges

Low Input Bias and Offset Currents

Output Short-Circuit Protection

Low Total Harmonic Distortion . . . 0.003% Typ

Low Noise

V_n = 18 nV/√Hz Typ at f = 1 kHz

High Input Impedance . . . JFET Input Stage

Internal Frequency Compensation

Latch-Up-Free Operation

High Slew Rate . . . 13 V/μs Typ

Common-Mode Input Voltage Range Includes V_{CC+}

16. Contents

description/ordering information

The JFET input operational amplifiers in the TL07x series are similar to the TL08x series, with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07x series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

© Koninklijke Philips Electronics N.V. 2005

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Copyright © 2005, Texas Instruments Incorporated

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Date of release: 19 May 2005
Document number: 9397 750 14609

Published in The Netherlands

description/ordering information (continued)

ORDERING INFORMATION

T_A	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	10 mV	PDIP (P)	Tube of 50	TL071CP	TL071CP
			Tube of 50	TL072CP	TL072CP
		PDIP (N)	Tube of 25	TL074CN	TL074CN
		SOIC (D)	Tube of 75	TL071CD	TL071C
			Reel of 2500	TL071CDR	
			Tube of 75	TL072CD	TL072C
			Reel of 2500	TL072CDR	
			Tube of 50	TL074CD	TL074C
			Reel of 2500	TL074CDR	
		SOP (NS)	Reel of 2000	TL074CNSR	TL074
		SOP (PS)	Reel of 2000	TL071CPSR	TL071
			Reel of 2000	TL072CPSR	T072
		TSSOP (PW)	Reel of 2000	TL072CPWR	T072
			Tube of 90	TL074CPW	T074
			Reel of 2000	TL074CPWR	
	6 mV	PDIP (P)	Tube of 50	TL071ACP	TL071ACP
			Tube of 50	TL072ACP	TL072ACP
		PDIP (N)	Tube of 25	TL074ACN	TL074ACN
		SOIC (D)	Tube of 75	TL071ACD	071AC
			Reel of 2500	TL071ACDR	
			Tube of 75	TL072ACD	072AC
			Reel of 2500	TL072ACDR	
			Tube of 50	TL074ACD	TL074AC
			Reel of 2500	TL074ACDR	
		SOP (PS)	Reel of 2000	TL072ACPSR	T072A
		SOP (NS)	Reel of 2000	TL074ACNSR	TL074A
	3 mV	PDIP (P)	Tube of 50	TL071BCP	TL071BCP
			Tube of 50	TL072BCP	TL072BCP
		PDIP (N)	Tube of 25	TL074BCN	TL074BCN
		SOIC (D)	Tube of 75	TL071BCD	071BC
			Reel of 2500	TL071BCDR	
			Tube of 75	TL072BCD	072BC
			Reel of 2500	TL072BCDR	
			Tube of 50	TL074BCD	TL074BC
			Reel of 2500	TL074BCDR	
		SOP (NS)	Reel of 2000	TL074BCNSR	TL074B

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

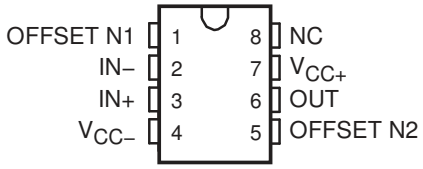
description/ordering information (continued)

ORDERING INFORMATION

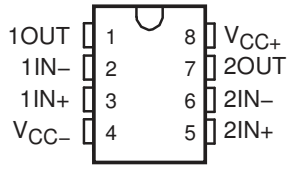
T_A	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	6 mV	PDIP (P)	Tube of 50	TL071IP	TL071IP
			Tube of 50	TL072IP	TL072IP
		PDIP (N)	Tube of 25	TL074IN	TL074IN
		SOIC (D)	Tube of 75	TL071ID	TL071I
			Reel of 2500	TL071IDR	
			Tube of 75	TL072ID	TL072I
			Reel of 2500	TL072IDR	
			Tube of 50	TL074ID	TL074I
			Reel of 2500	TL074IDR	
–55°C to 125°C	6 mV	CDIP (JG)	Tube of 50	TL072MJGB	TL072MJGB
		CFP (U)	Tube of 150	TL072MUB	TL072MUB
		LCCC (FK)	Tube of 55	TL072MFKB	TL072MFKB
	9 mV	CDIP (J)	Tube of 25	TL074MJB	TL074MJB
		CFP (W)	Tube of 25	TL074MWB	TL074MWB
		LCCC (FK)	Tube of 55	TL074MFKB	TL074MFKB

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

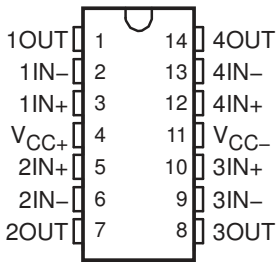
TL071, TL071A, TL071B
D, P, OR PS PACKAGE
(TOP VIEW)



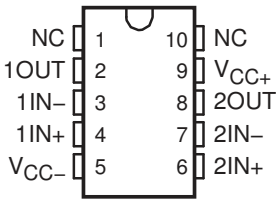
TL072, TL072A, TL072B
D, JG, P, PS, OR PW PACKAGE
(TOP VIEW)



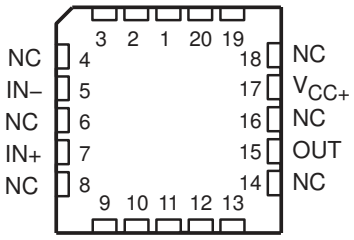
TL074A, TL074B
D, J, N, NS, OR PW PACKAGE
TL074 . . . D, J, N, NS, PW,
OR W PACKAGE
(TOP VIEW)



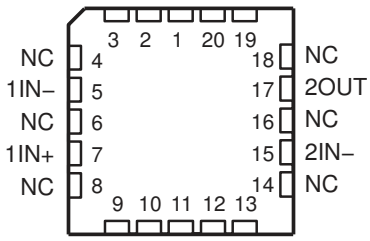
TL072
U PACKAGE
(TOP VIEW)



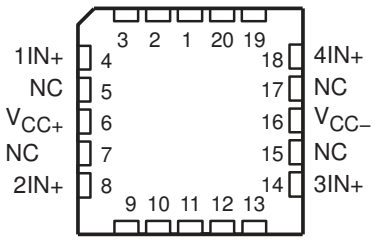
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)



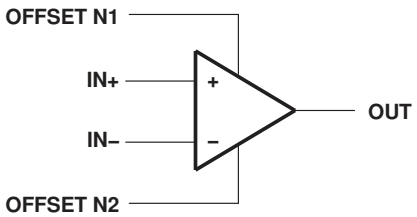
TL074
FK PACKAGE
(TOP VIEW)



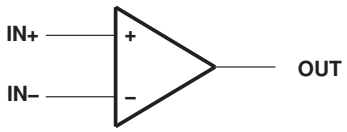
NC – No internal connection

symbols

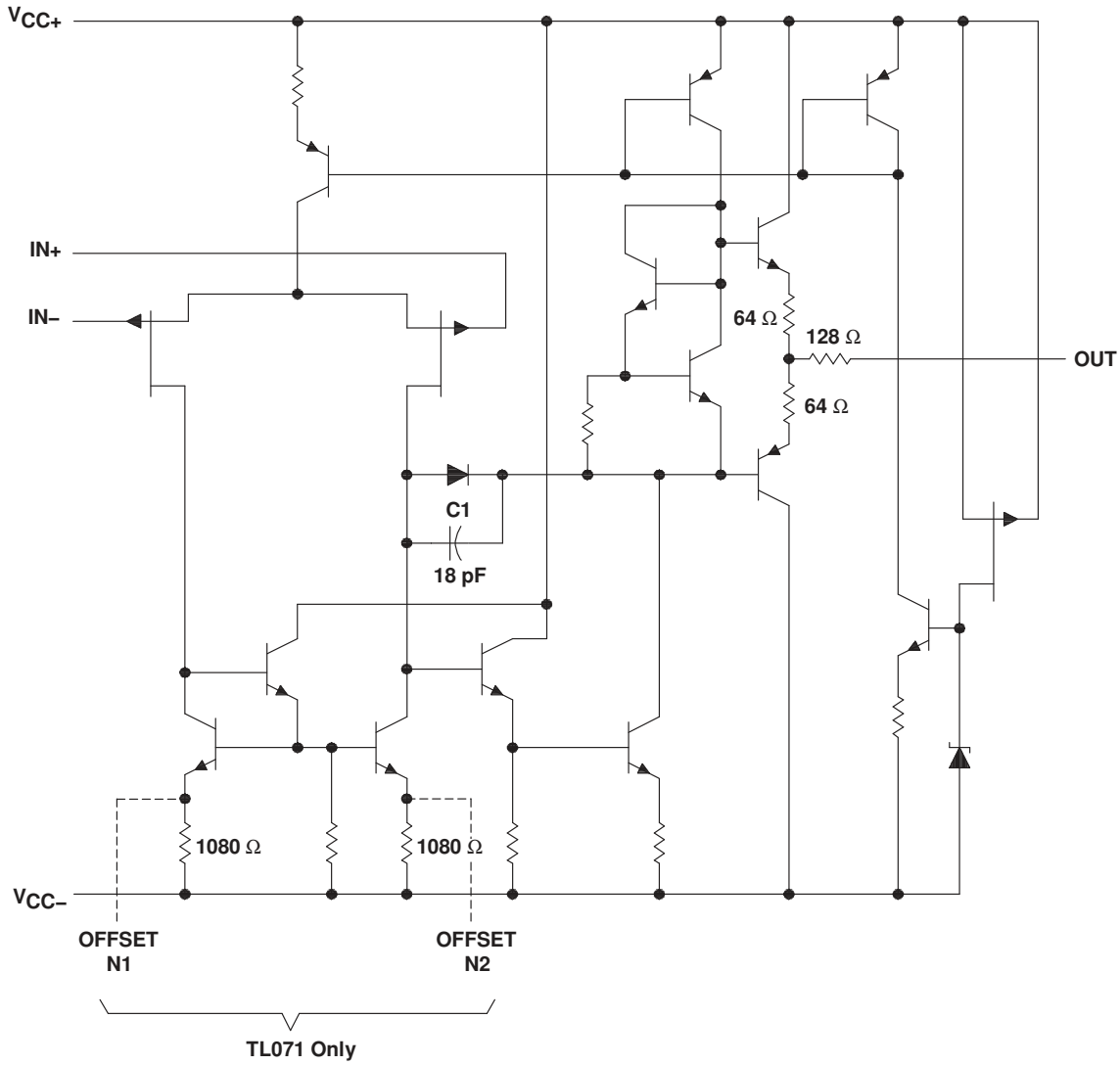
TL071



TL072 (each amplifier)
TL074 (each amplifier)



schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	**TL071**	**TL072**	**TL074**
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

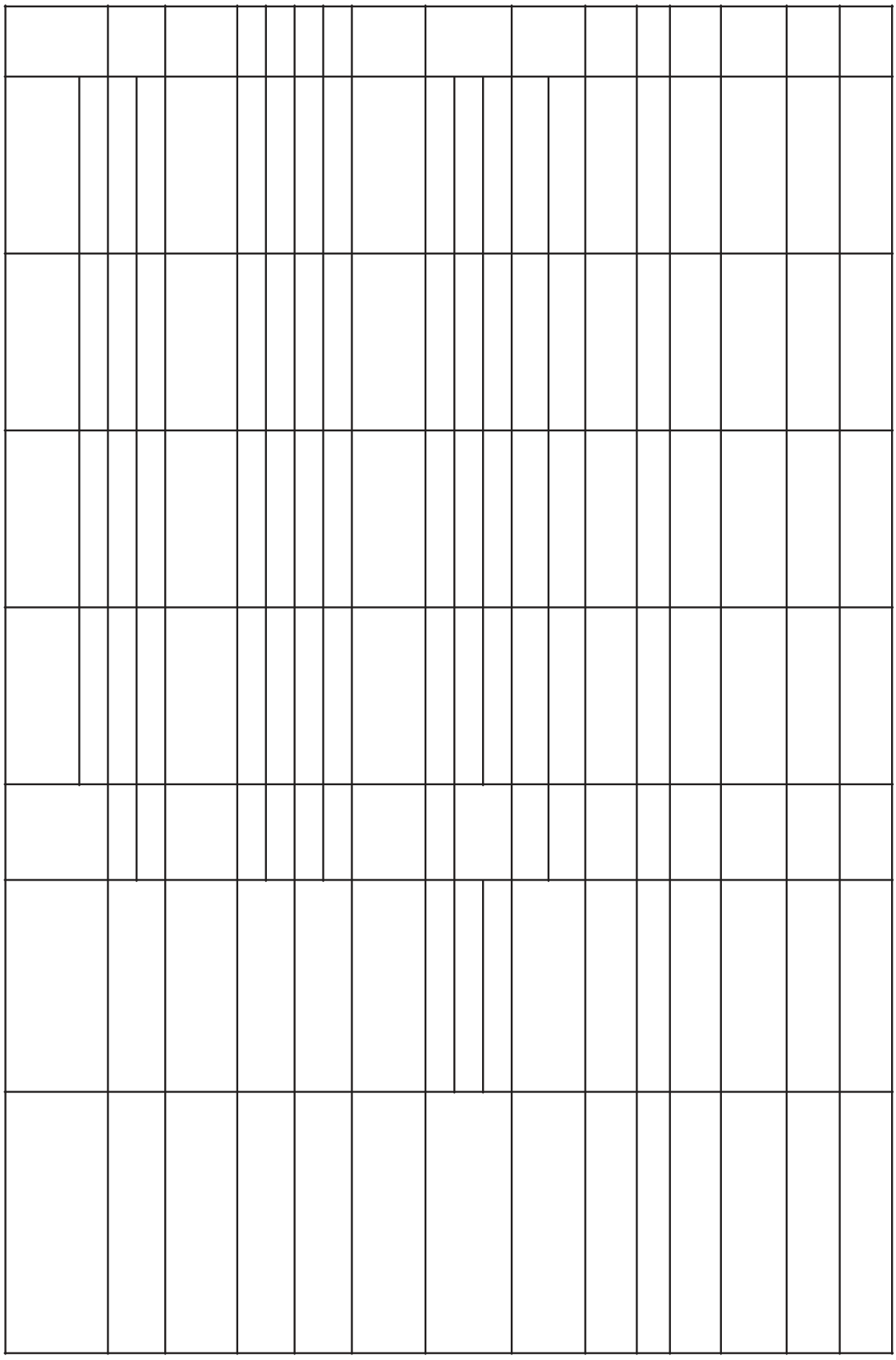
† Includes bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+}		18 V
V_{CC-}		–18 V
Differential input voltage, V_{ID} (see Note 2)		±30 V
Input voltage, V_I (see Notes 1 and 3)		±15 V
Duration of output short circuit (see Note 4)		Unlimited
Package thermal impedance, θ_{JA} (see Notes 5 and 6):	D package (8 pin)	97°C/W
	D package (14 pin)	86°C/W
	N package	80°C/W
	NS package	76°C/W
	P package	85°C/W
	PS package	95°C/W
	PW package (8 pin)	149°C/W
	PW package (14 pin)	113°C/W
	U package	185°C/W
Package thermal impedance, θ_{JC} (see Notes 7 and 8):	FK package	5.61°C/W
	J package	15.05°C/W
	JG package	14.5°C/W
	W package	14.65°C/W
Operating virtual junction temperature, T_J		150°C
Case temperature for 60 seconds: FK package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or W package		300°C
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+, with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.
7. Maximum power dissipation is a function of $T_J(max)$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) – T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
8. The package thermal impedance is calculated in accordance with MIL-STD-883.



electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18		µV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100	pA
			Full range			20			20	nA
I_{IB}	Input bias current‡	V_O = 0	25°C		65	200		65	200	pA
						50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	35	200		35	200		V/mV
				15			15			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

† Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡ All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is T_A = –55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TL07xM			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	5	13		8	13		V/μs
t_r	Rise-time overshoot factor	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.1			0.1		μs
					20%			20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		μV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, $R_L \geq$ 2 kΩ, f = 1 kHz	A_{VD} = 1, R ≤ 1 kΩ,		0.003 %			0.003%		

PARAMETER MEASUREMENT INFORMATION

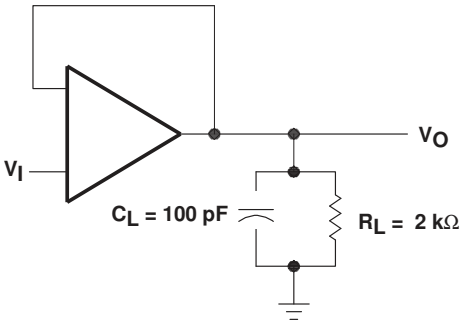


Figure 1. Unity-Gain Amplifier

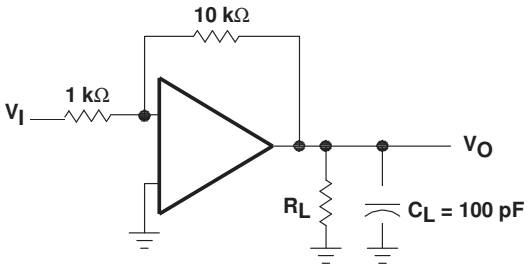


Figure 2. Gain-of-10 Inverting Amplifier

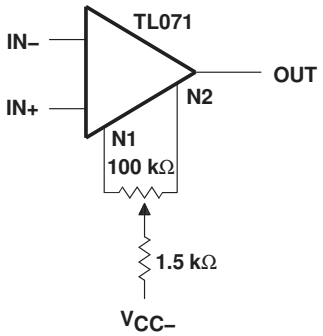


Figure 3. Input Offset-Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	4
V_{OM}	Maximum output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Phase shift	vs Frequency	12
	Normalized unity-gain bandwidth	vs Free-air temperature	13
	Normalized phase shift	vs Free-air temperature	13
CMRR	Common-mode rejection ratio	vs Free-air temperature	14
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	15 16
P_D	Total power dissipation	vs Free-air temperature	17
	Normalized slew rate	vs Free-air temperature	18
V_n	Equivalent input noise voltage	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20
	Large-signal pulse response	vs Time	21
V_O	Output voltage	vs Elapsed time	22

TYPICAL CHARACTERISTICS†

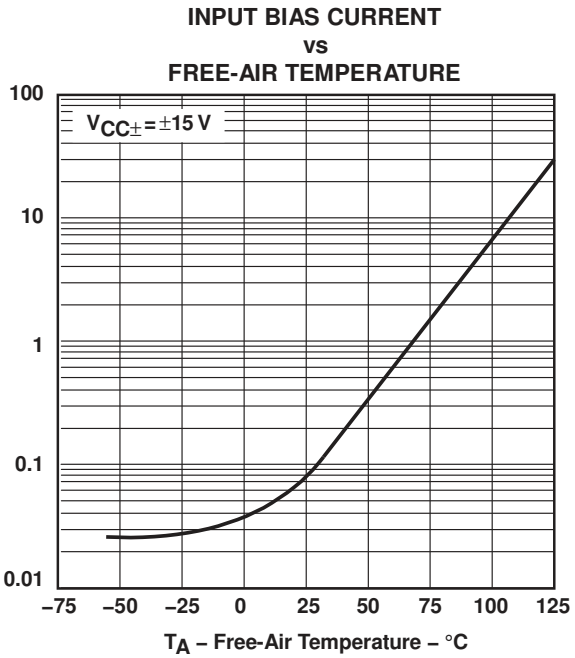


Figure 4

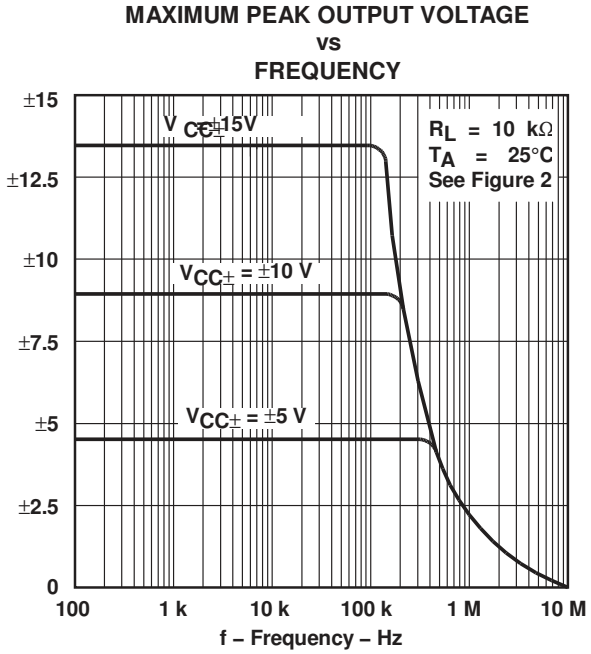


Figure 5

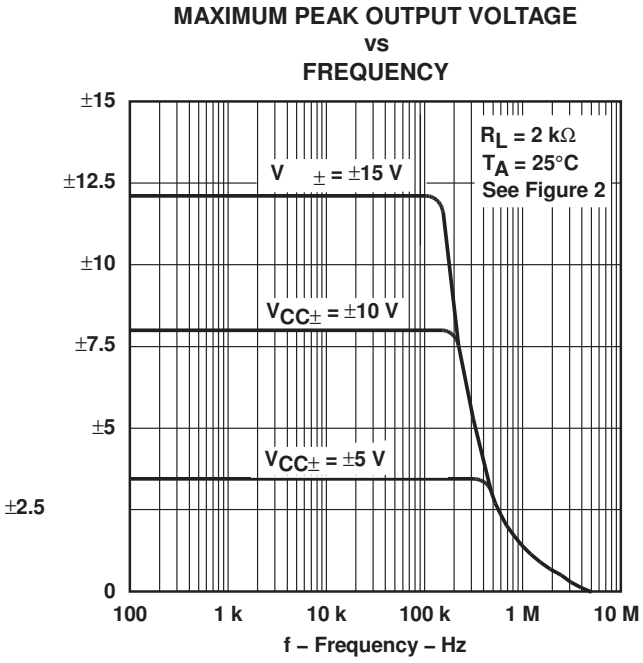


Figure 6

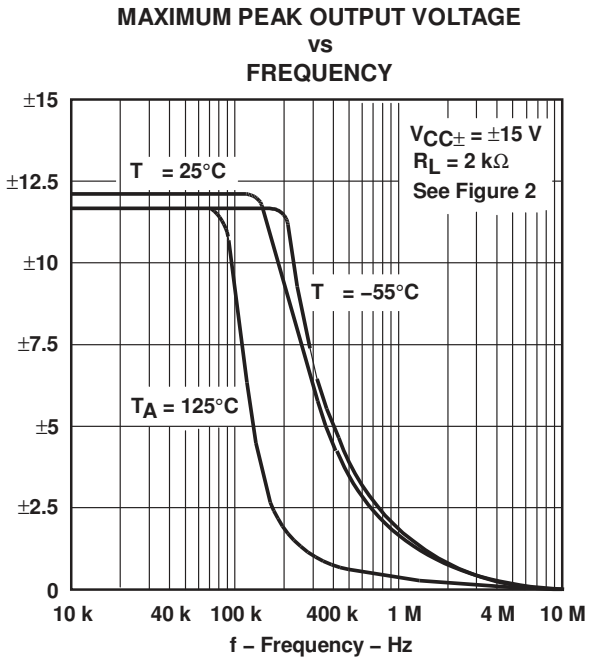


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

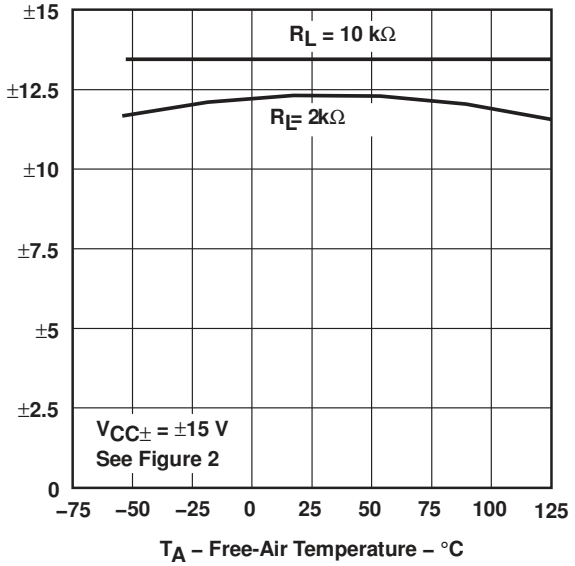


Figure 8

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

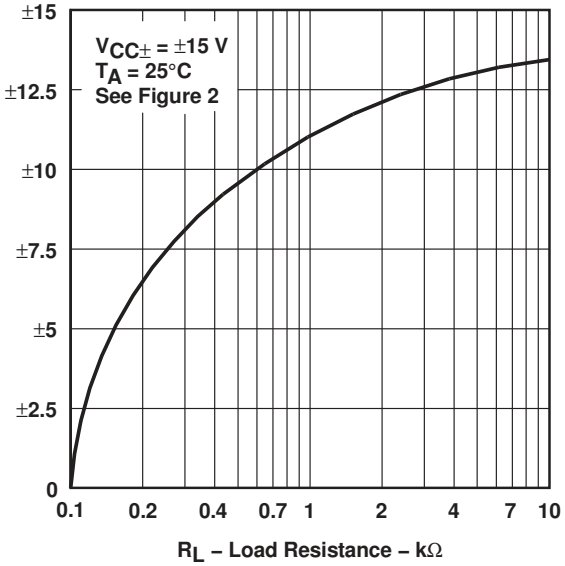


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

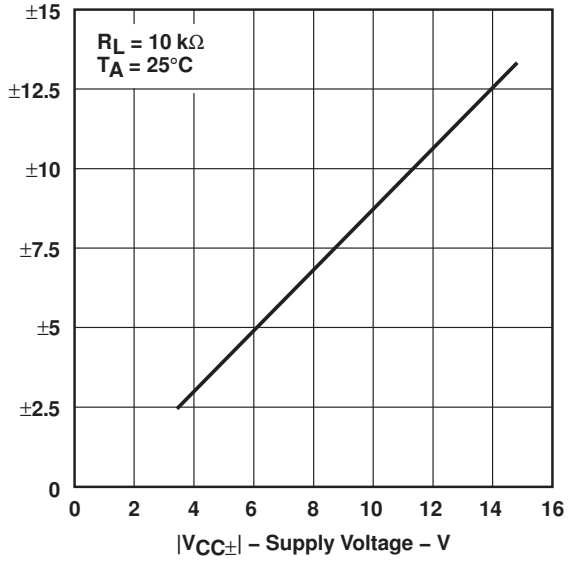


Figure 10

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

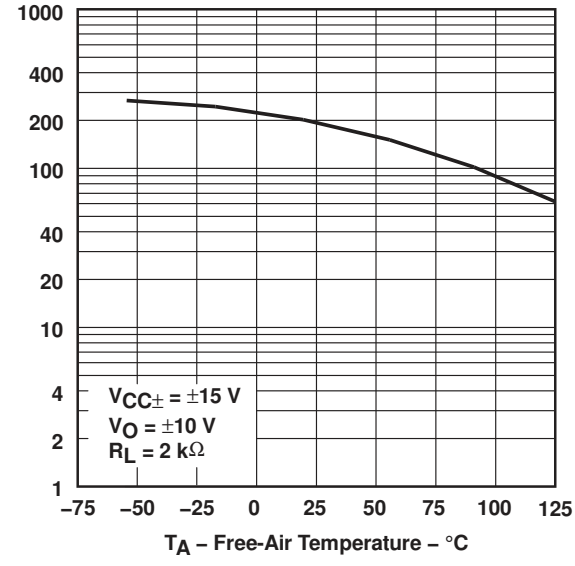


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

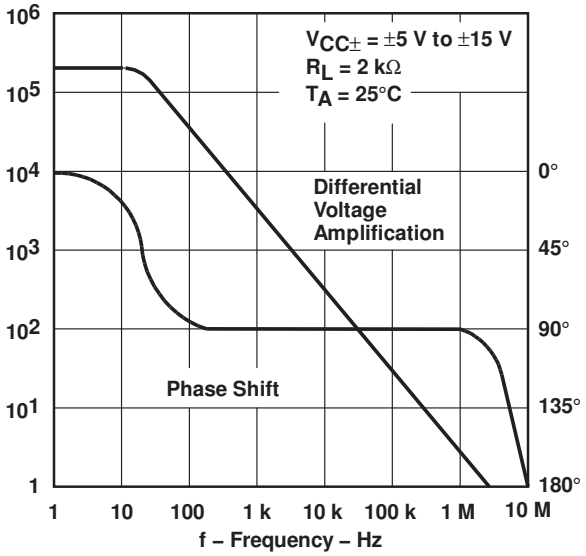


Figure 12

NORMALIZED UNITY-GAIN BANDWIDTH AND PHASE SHIFT vs FREE-AIR TEMPERATURE

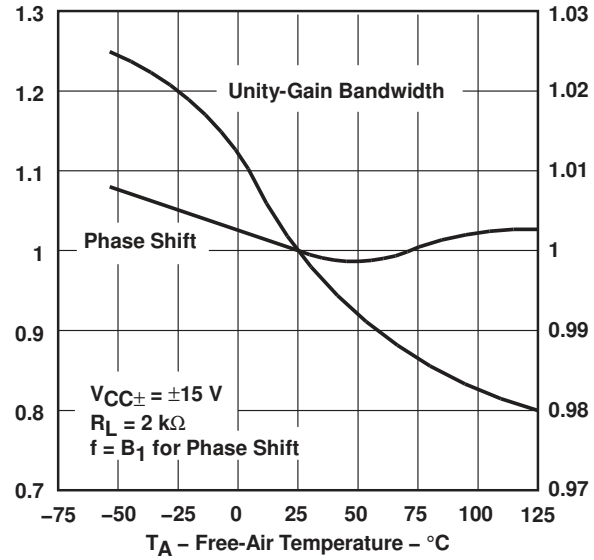


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

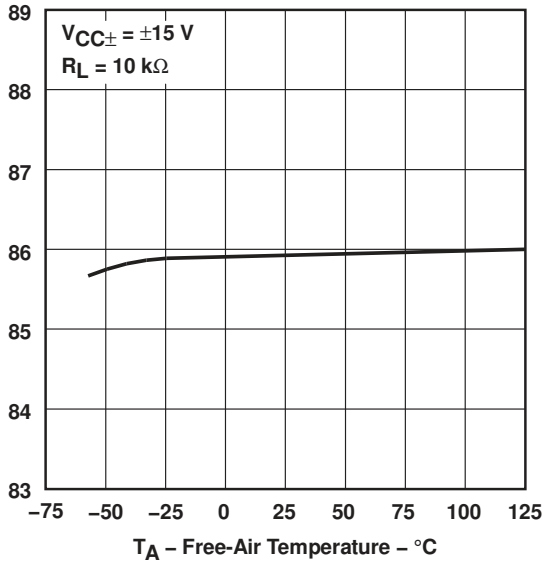


Figure 14

SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

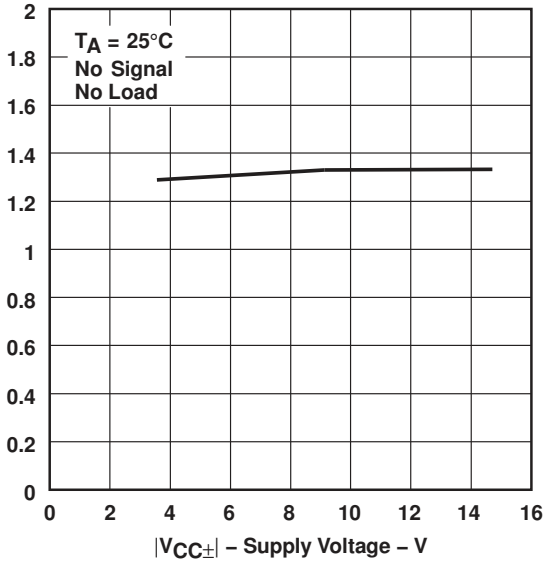


Figure 15

SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

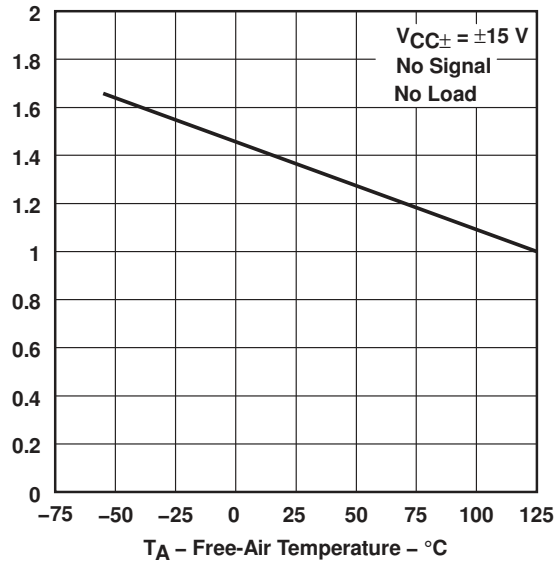


Figure 16

TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

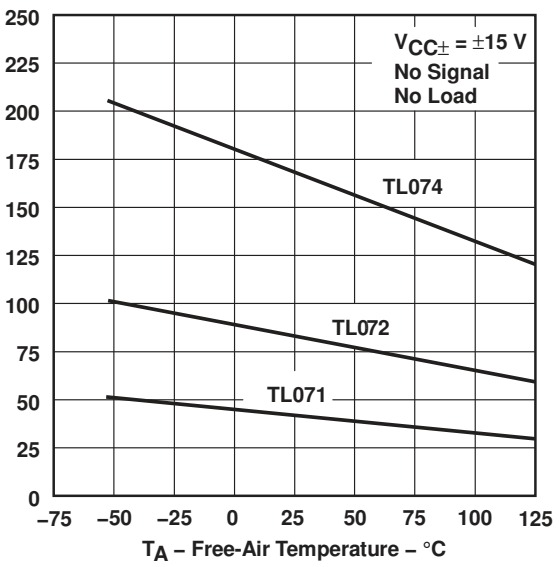


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

TYPICAL CHARACTERISTICS

NORMALIZED SLEW RATE vs FREE-AIR TEMPERATURE

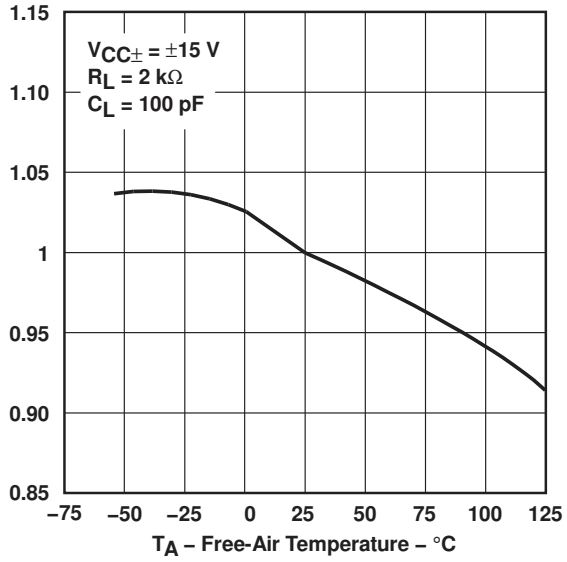


Figure 18

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

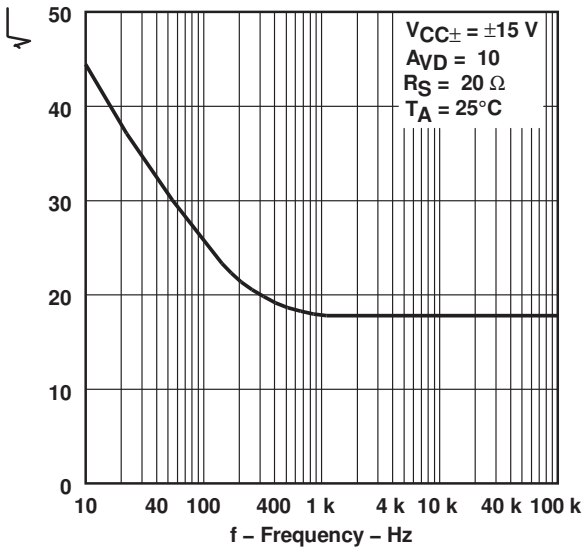


Figure 19

TOTAL HARMONIC DISTORTION vs FREQUENCY

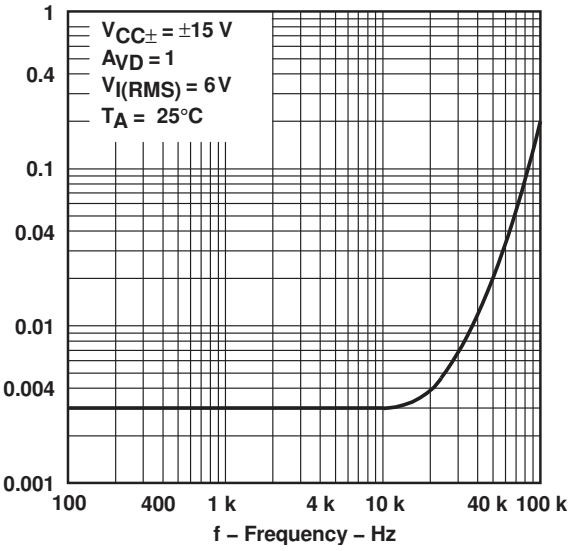


Figure 20

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

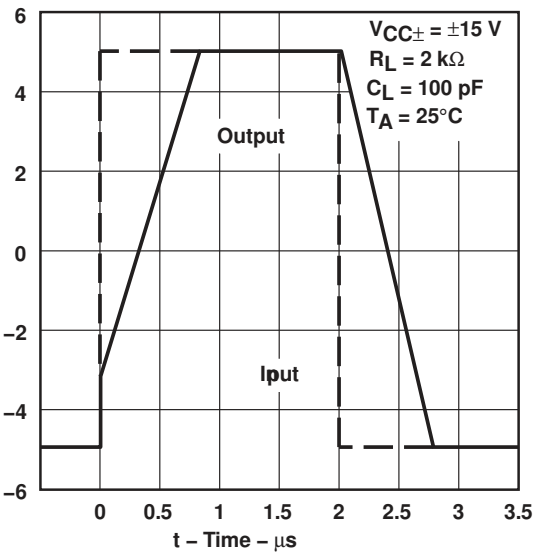


Figure 21

TYPICAL CHARACTERISTICS

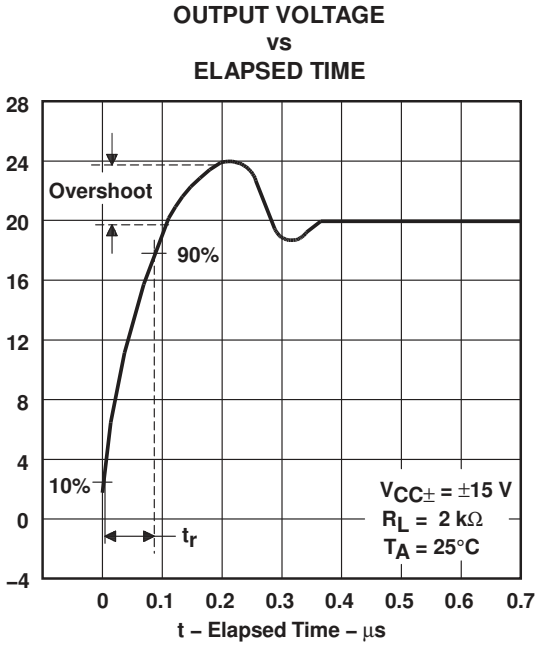


Figure 22

APPLICATION INFORMATION

Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
0.5-Hz square-wave oscillator	TL071	23
High-Q notch filter	TL071	24
Audio-distribution amplifier	TL074	25
100-kHz quadrature oscillator	TL072	26
AC amplifier	TL071	27

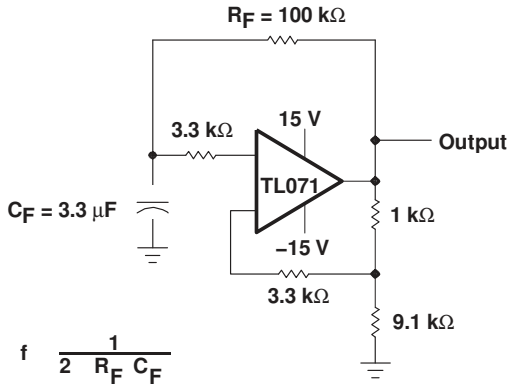


Figure 23. 0.5-Hz Square-Wave Oscillator

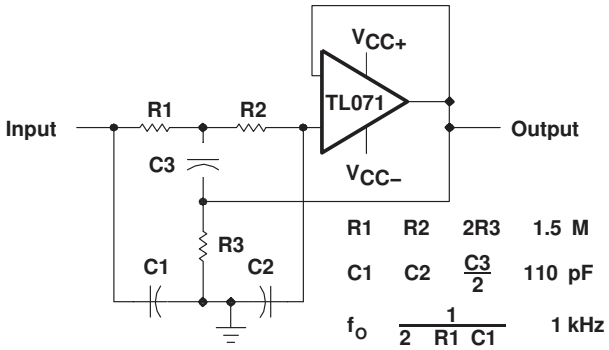


Figure 24. High-Q Notch Filter

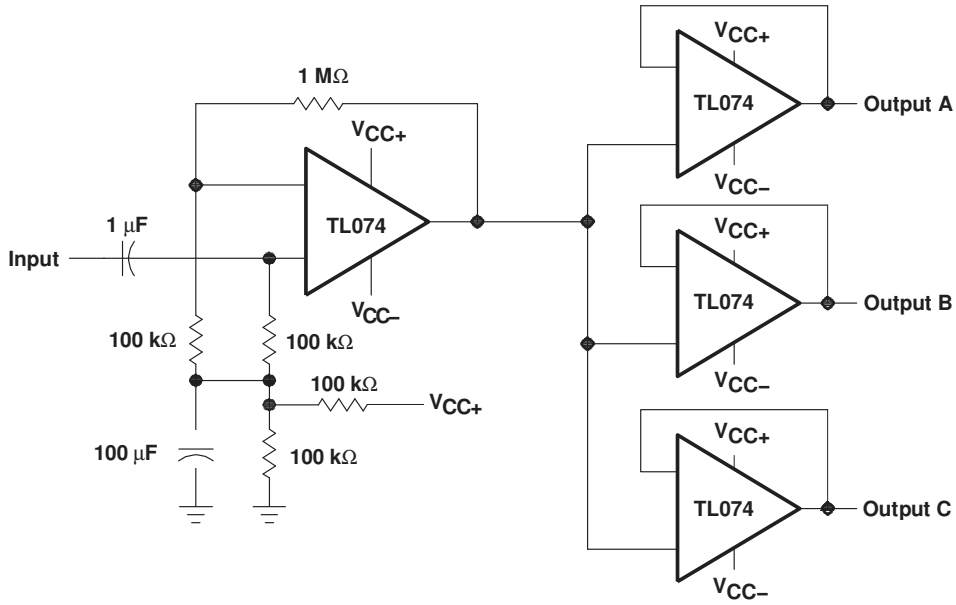
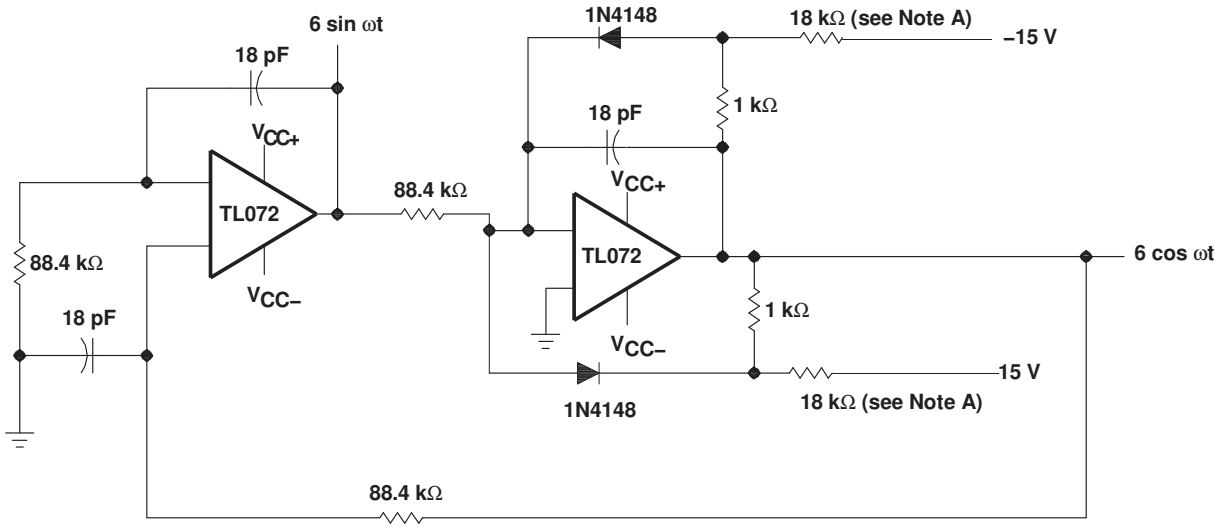


Figure 25. Audio-Distribution Amplifier

APPLICATION INFORMATION



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-kHz Quadrature Oscillator

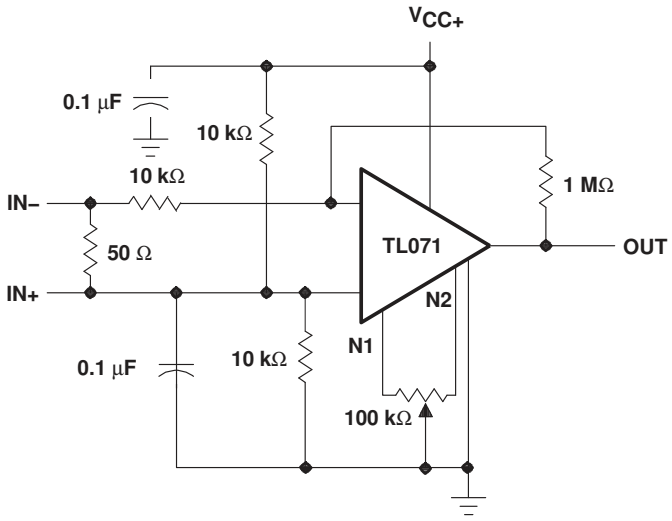


Figure 27. AC Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
8102304HA	OBSOLETE			10		TBD	Call TI	Call TI
81023052A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
8102305HA	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	Level-NC-NC-NC
8102305PA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
81023062A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
8102306CA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
8102306DA	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/11905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/11906BCA	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL071ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL071ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL071BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL071BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL071CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL071CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL071CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		
TL071CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TL071ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL071IJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL071IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL071IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL071MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
TL071MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL071MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL072ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072ACJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL072ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL072ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL072ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072ACPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL072BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL072CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS &	CU NIPDAU	Level-2-260C-1YEAR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		
TL072CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL072CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL072CPSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI
TL072CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL072ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
TL072IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL072IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL072MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TL072MJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TL072MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TL072MUB	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	Level-NC-NC-NC
TL074ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL074ACJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL074ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL074ACNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL074ACNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074ACNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074BCDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074BCDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL074BCNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL074BCNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074BCNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL074CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
TL074CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074CPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		
TL074IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL074IJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL074IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL074INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL074MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TL074MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TL074MJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
TL074MJB	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
TL074MWB	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

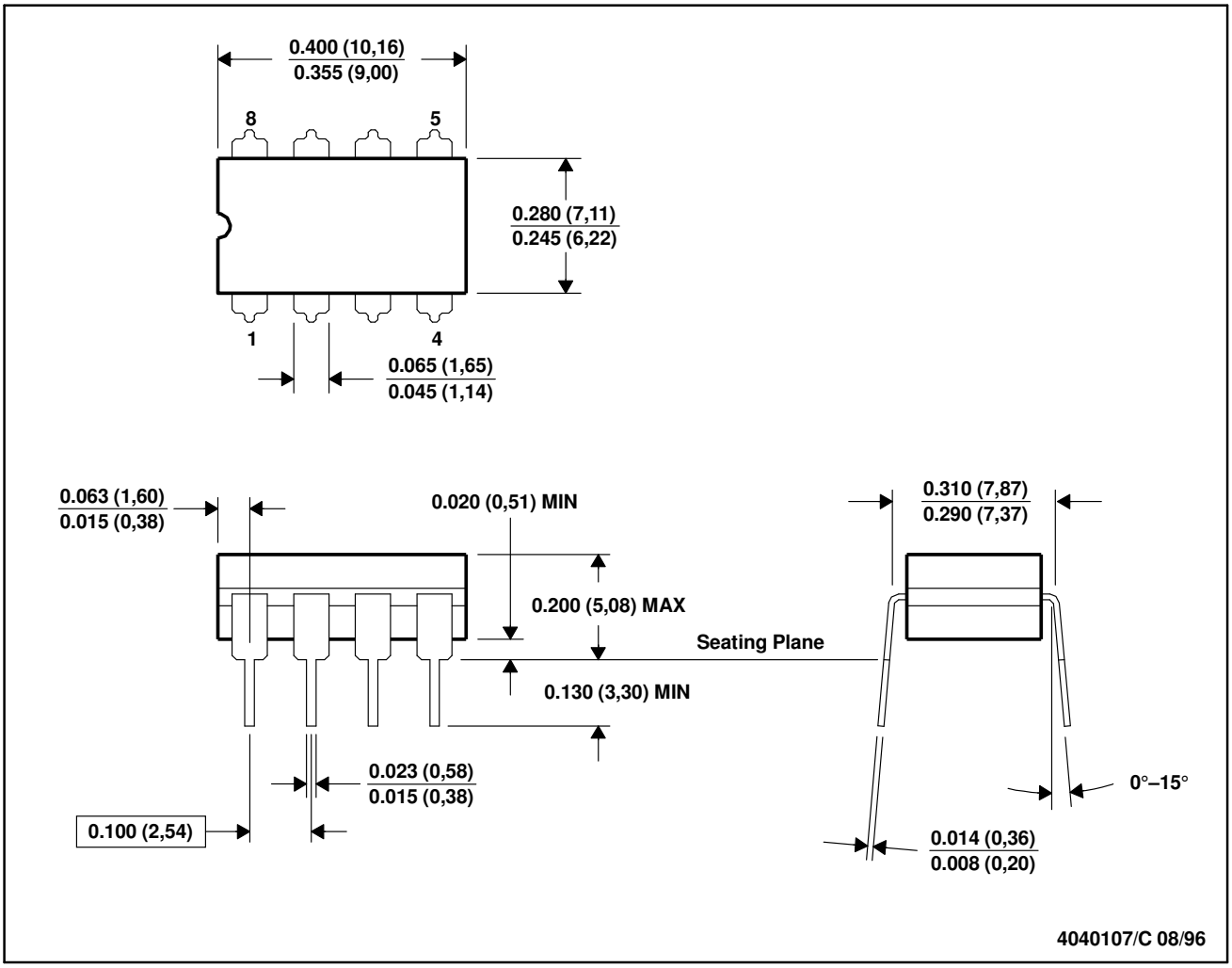
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

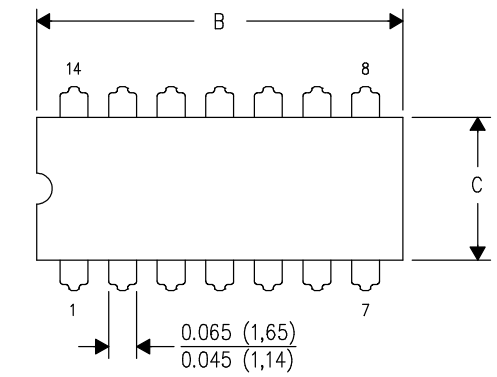
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



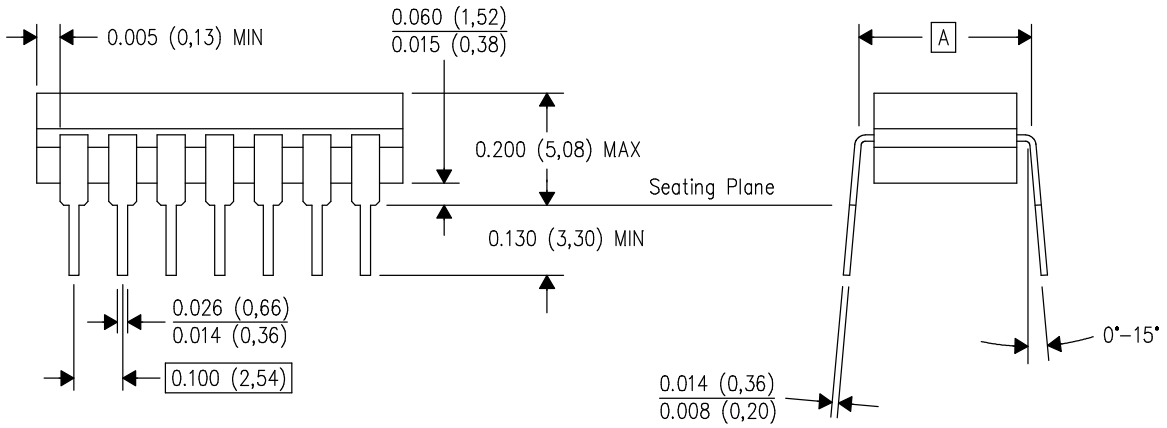
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



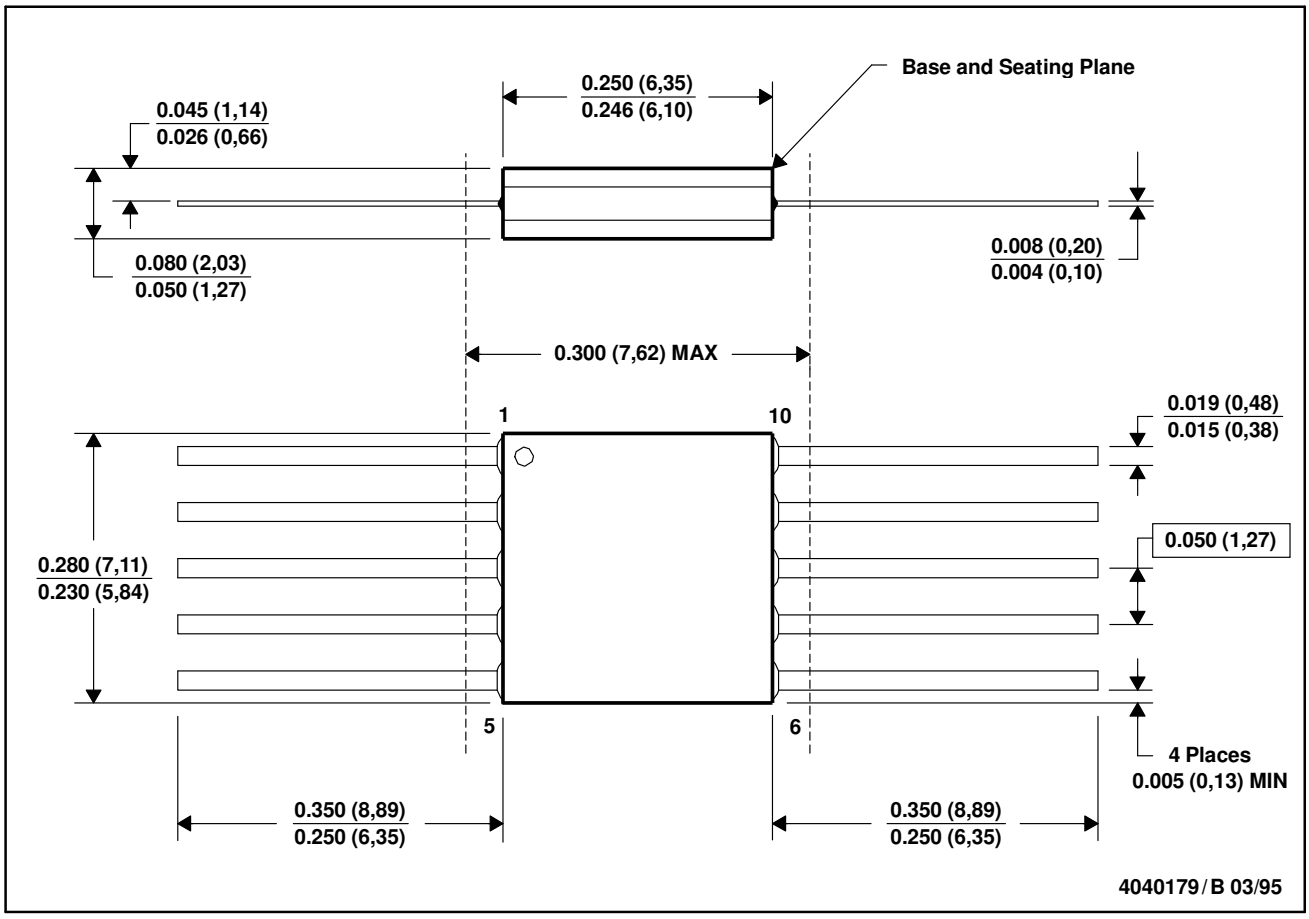
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

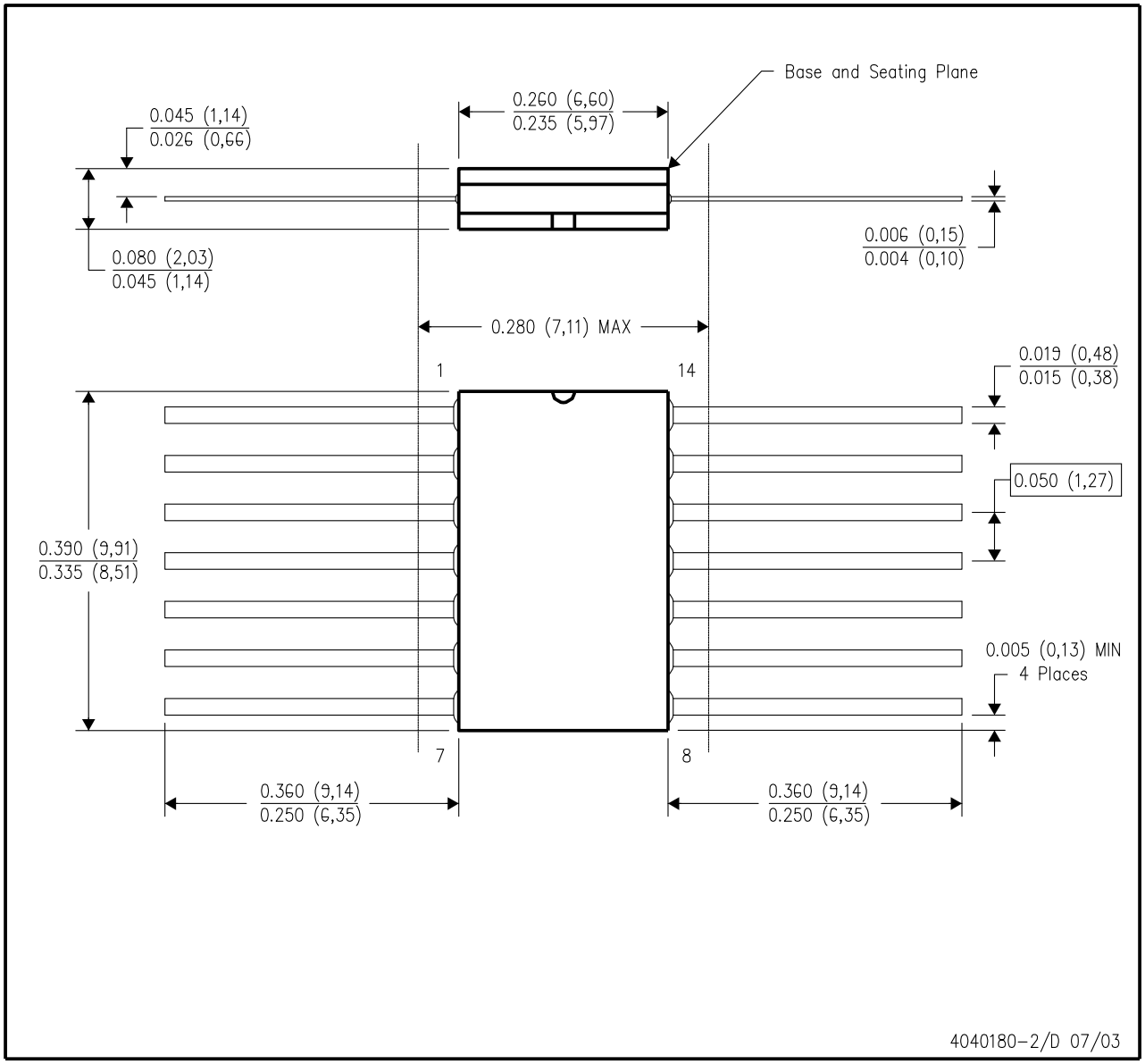
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

U (S-GDFP-F10) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

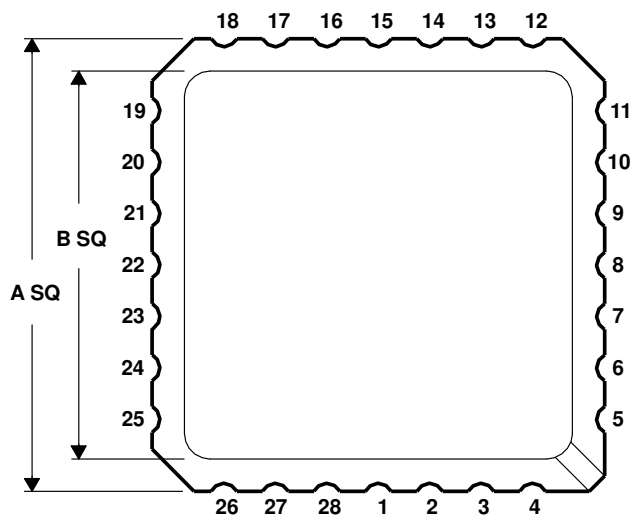
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



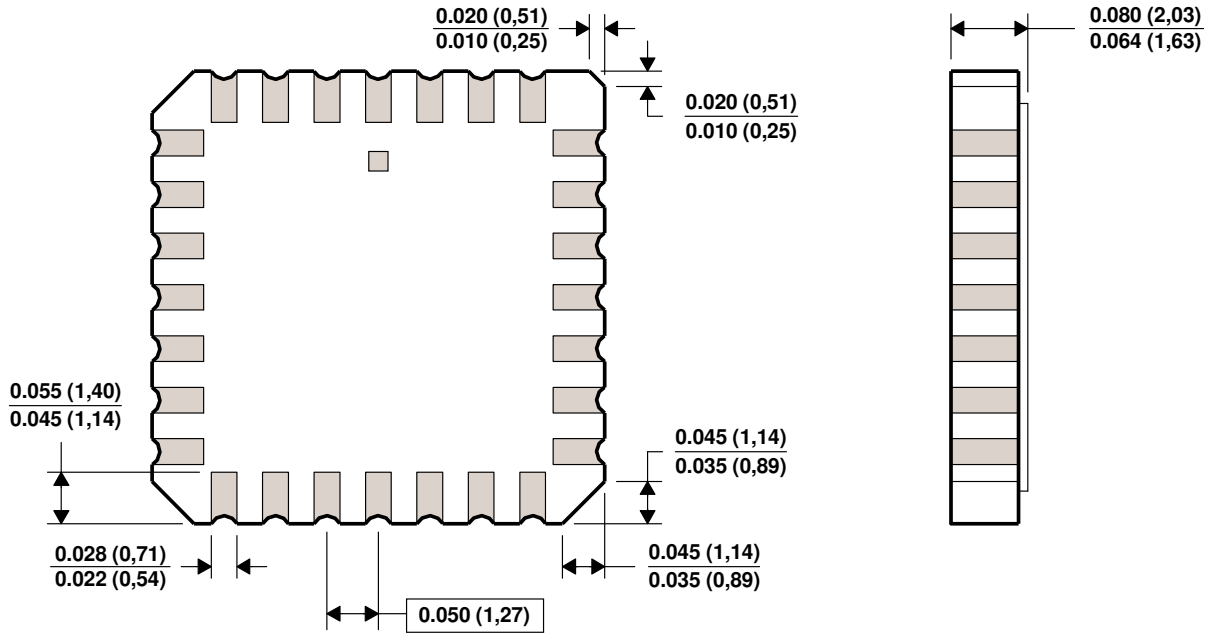
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

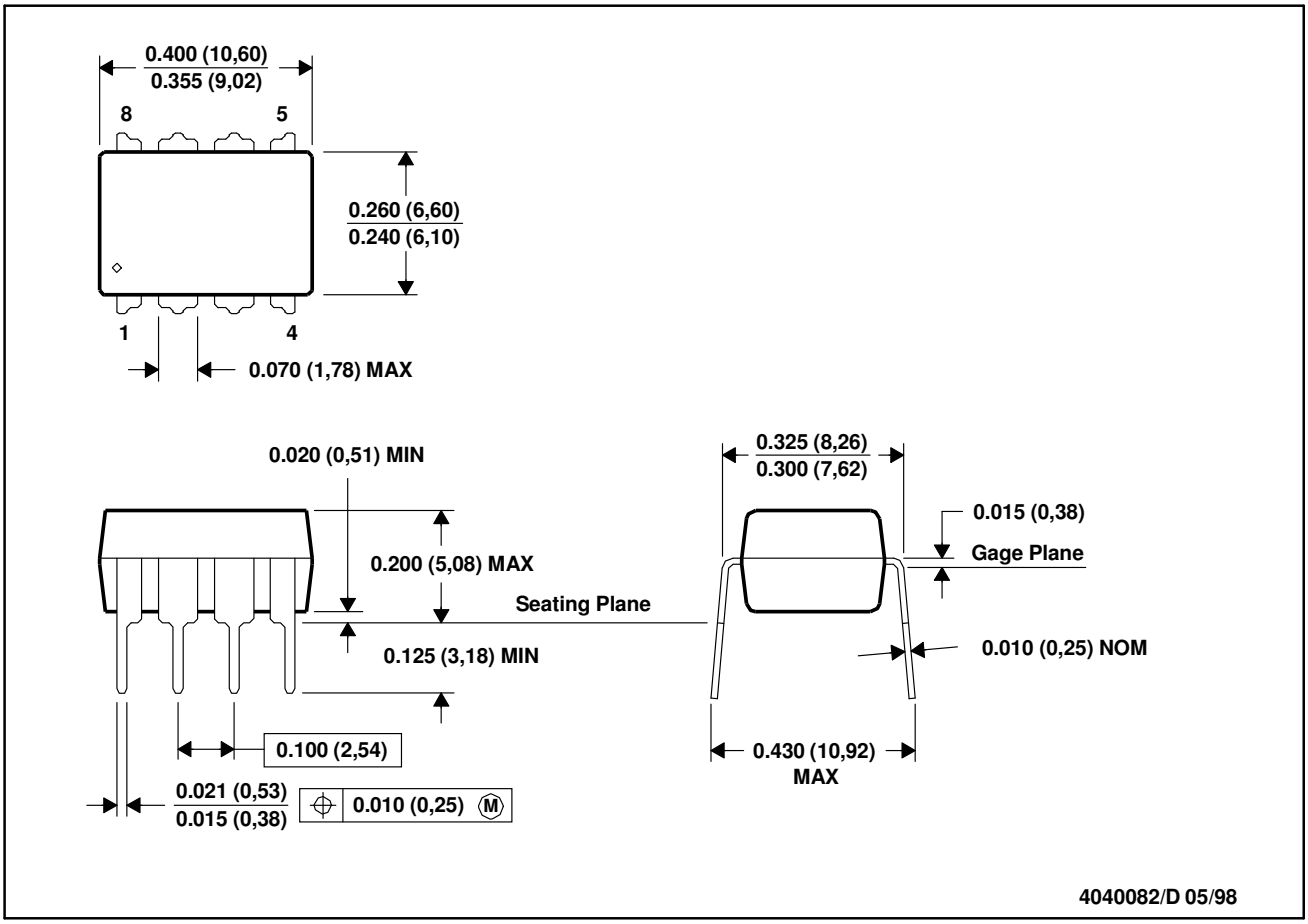


4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



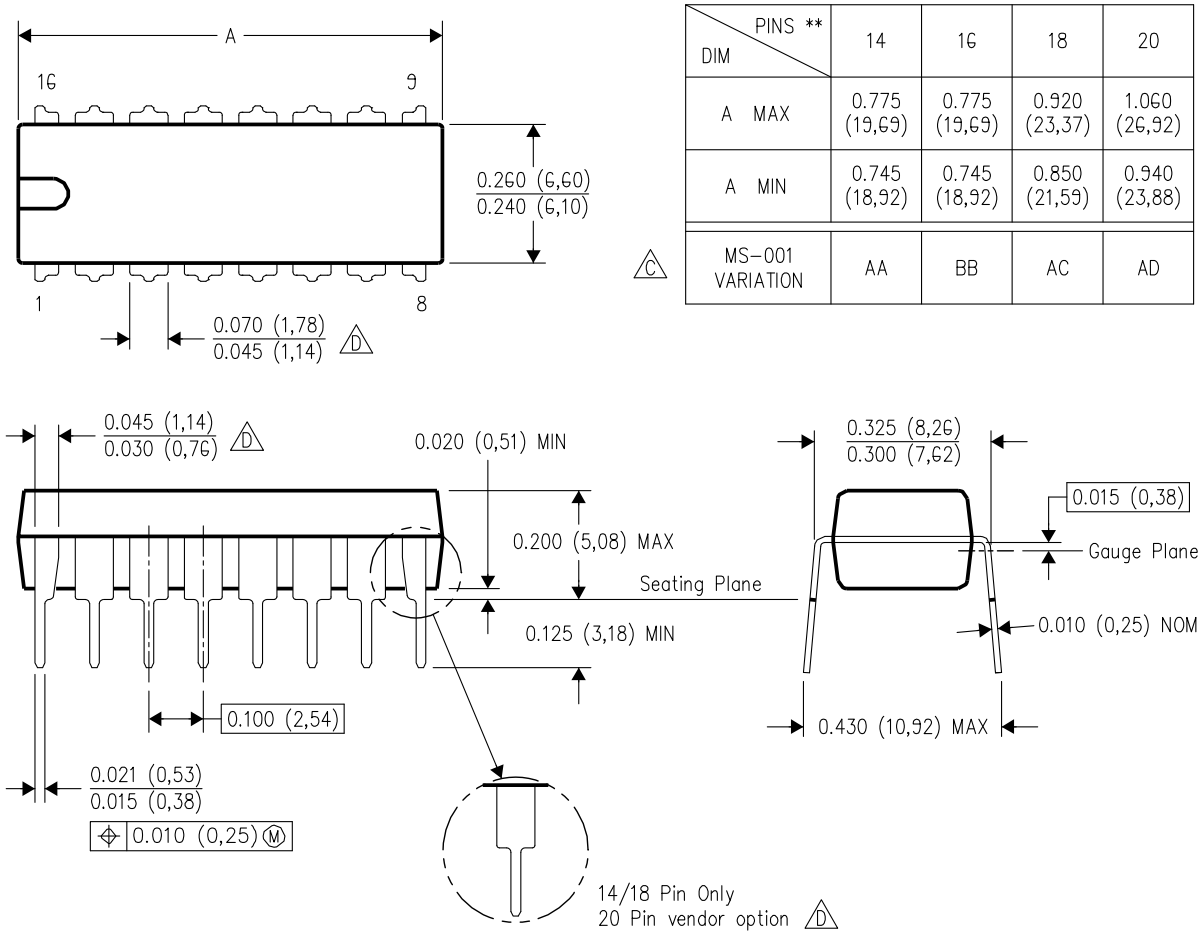
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



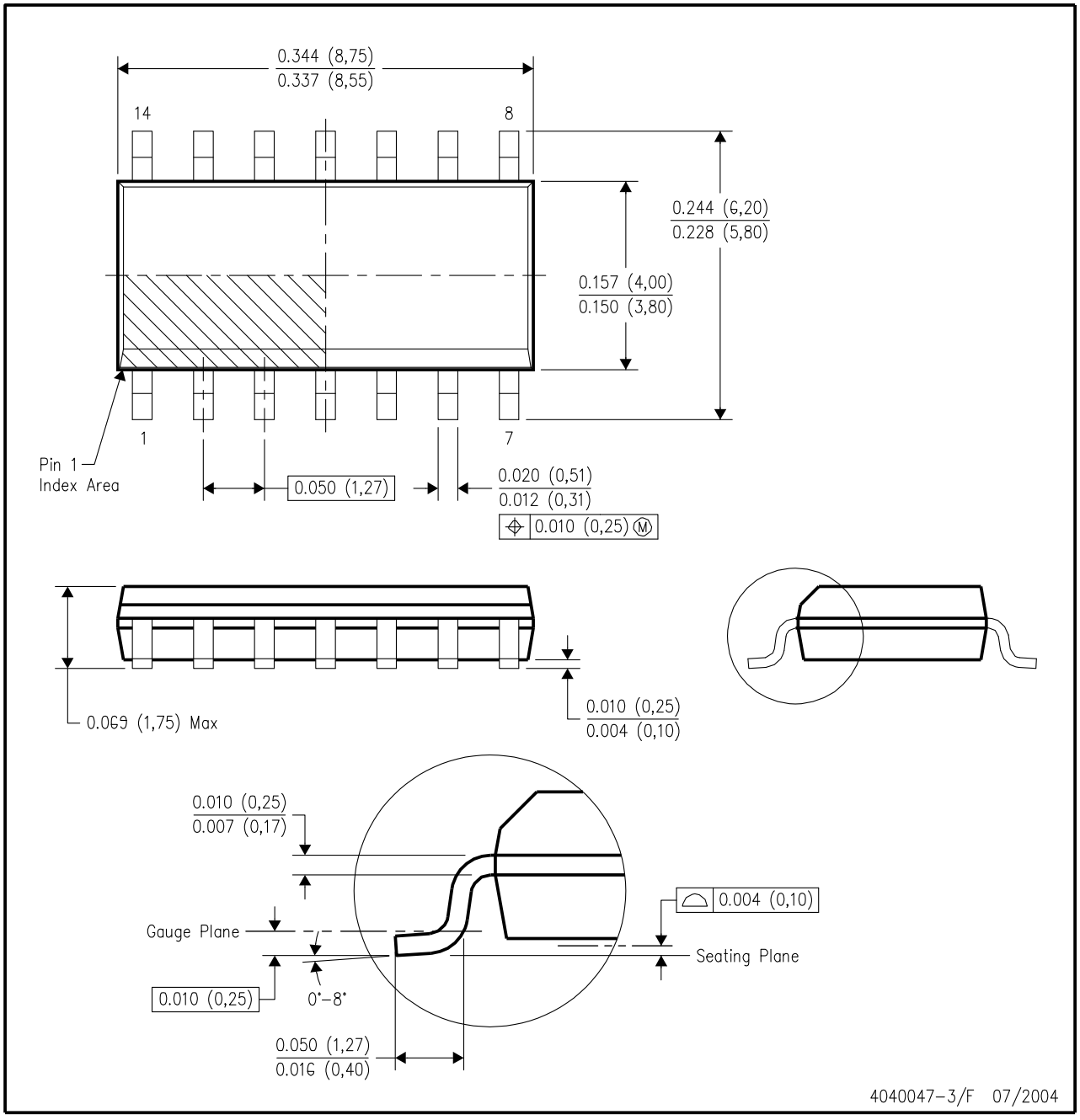
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

C

4040049/E 12/2002

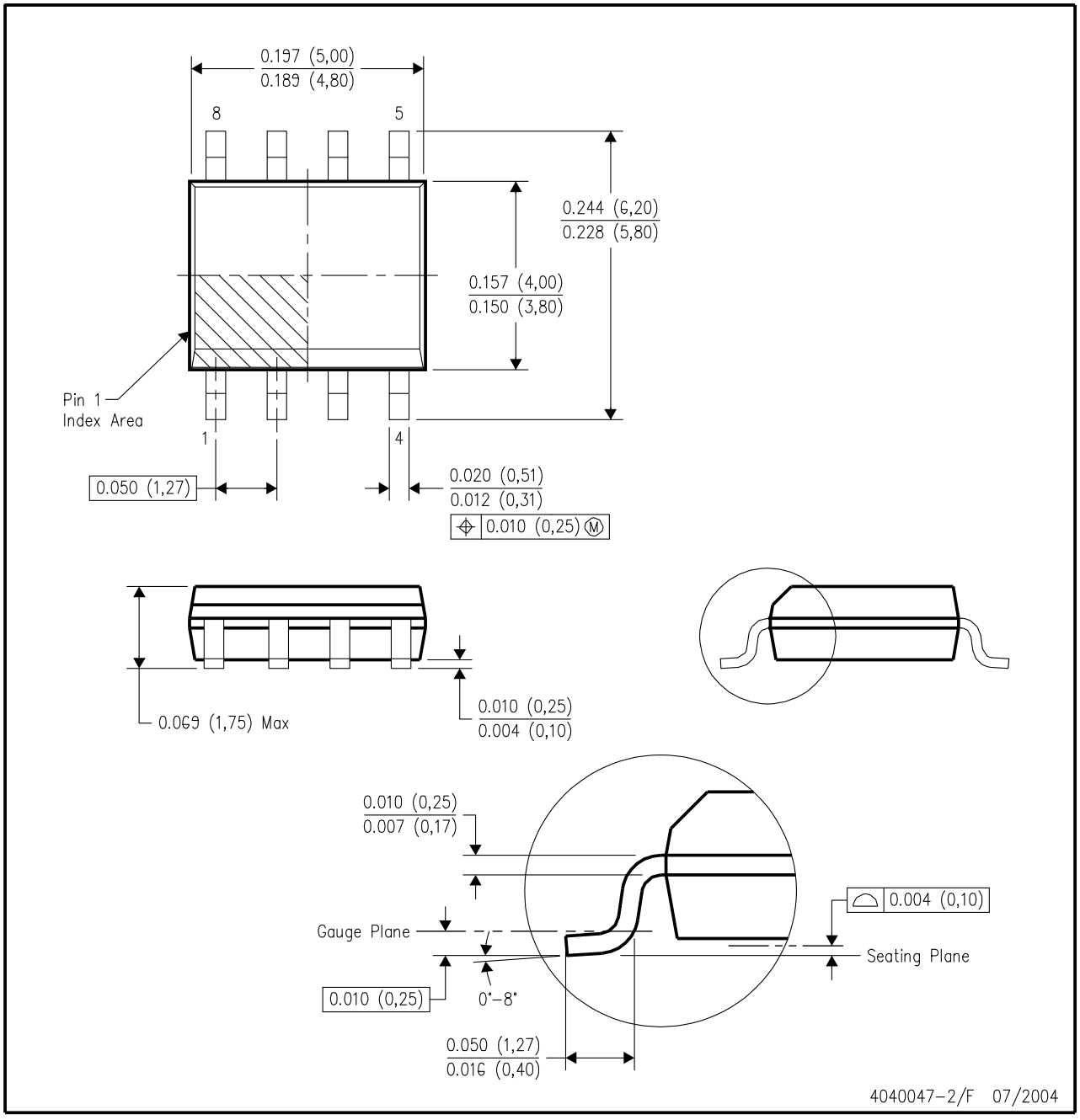
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

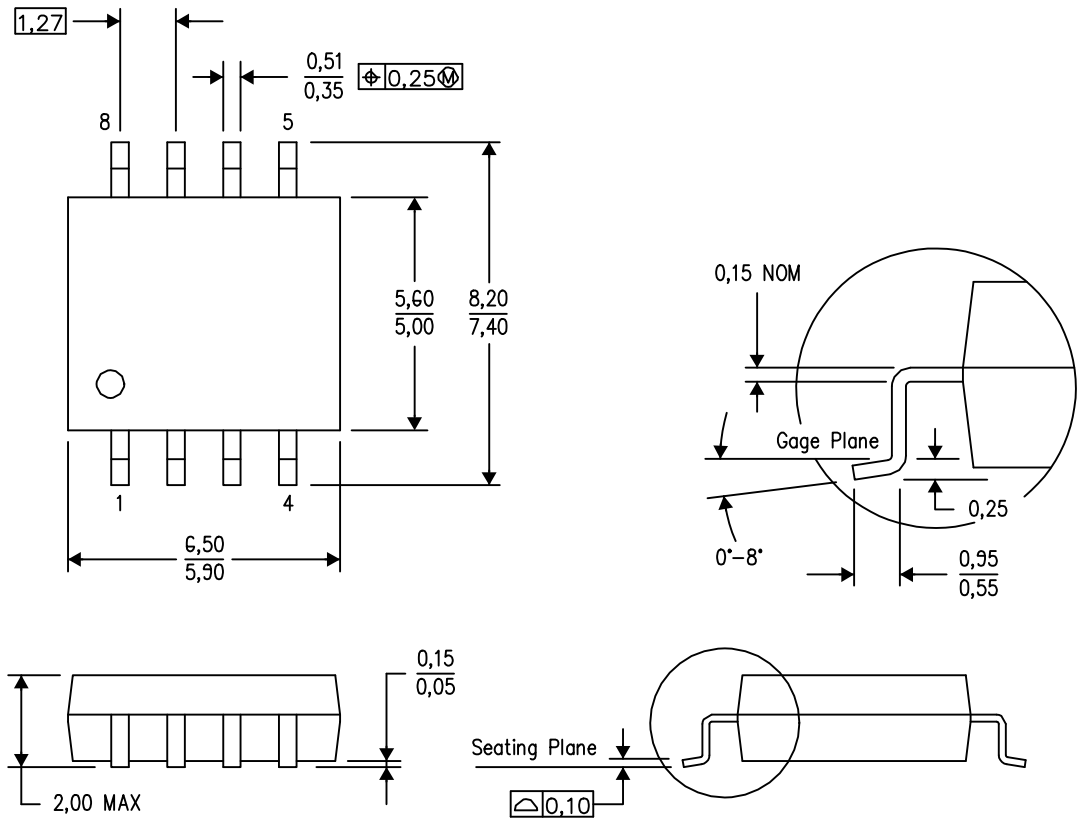
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

MECHANICAL DATA

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



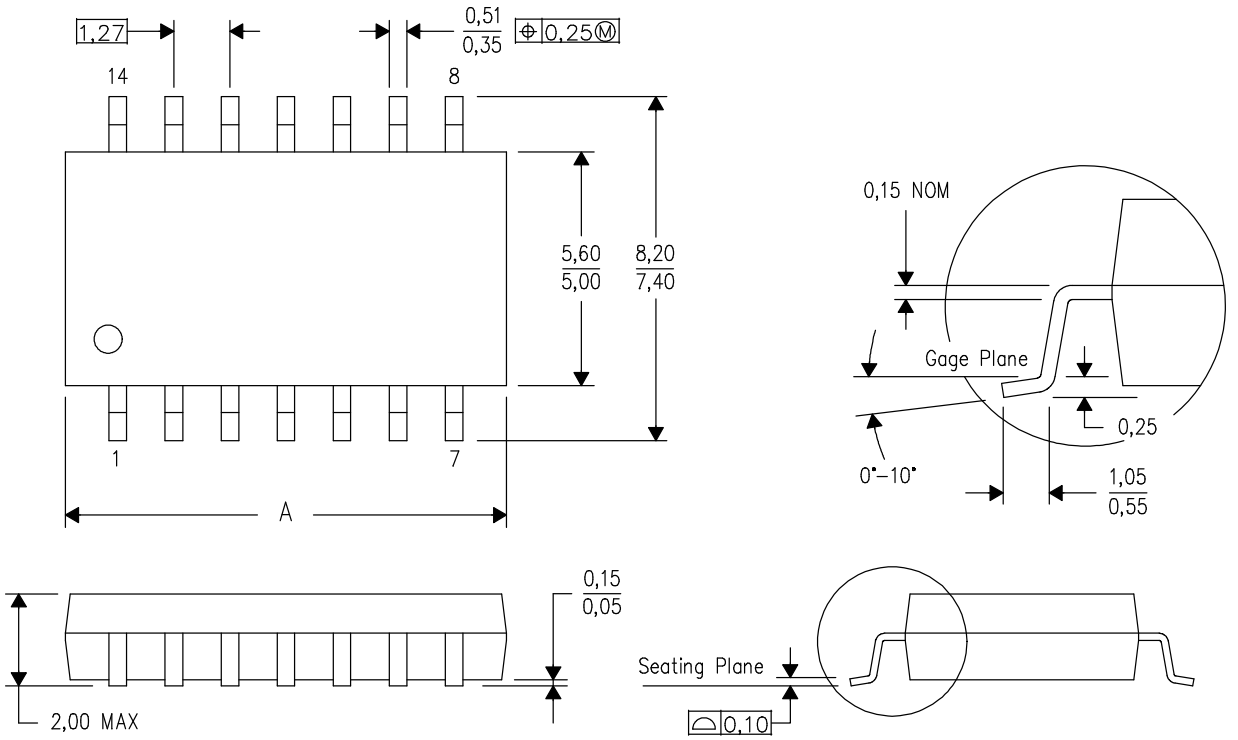
4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



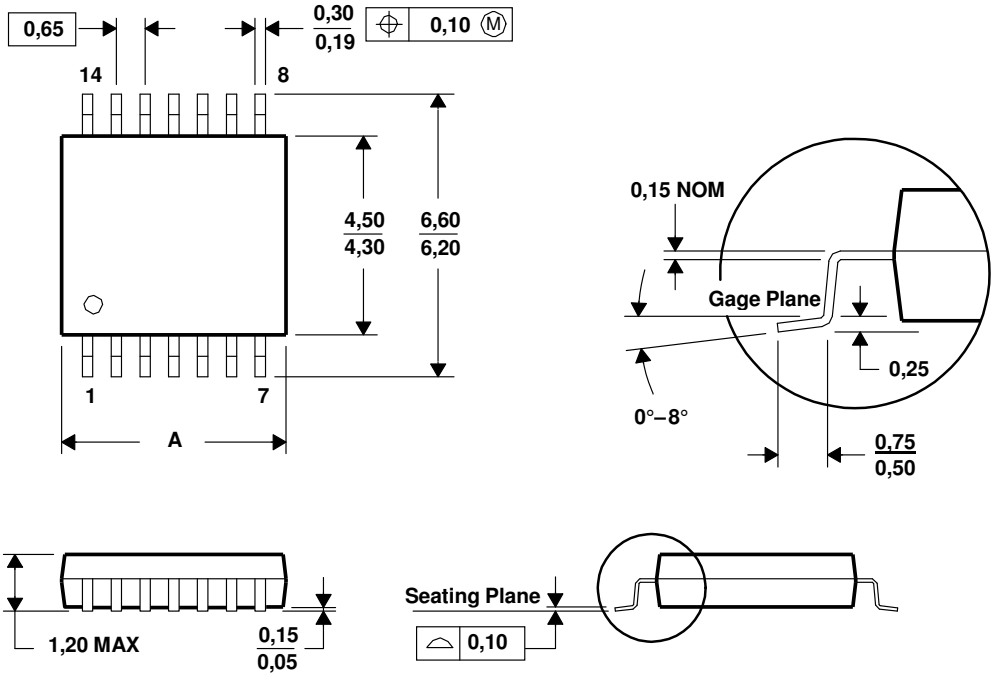
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated