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PAPER

Design of High-Speed High-Density Parallel Adders and Multipliers Using Regenerative Pass-Transistor Logic

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SUMMARY Regenerative Pass-transistor Logic (RPL), a modular dual-rail circuit technique for high speed logic design that gives reasonably low power consumption, was discussed in previous work [1]. RPL combines advantages of both the compact size of CPL and the full voltage-swing of DPL, and gives reasonably high performance concerning both speed and power consumption. In this paper, the application and design technique of RPL on larger logic circuits and systems are reported. Parallel adders and Booth multipliers with different sizes and structures are used as examples to evaluate the functionality of the RPL gates and full adder. In addition, there is less signal skew in RPL circuits than in conventional CPL circuits when an arrangement of single-rail to dual-rail signal conversion is performed. And, RPL is found to be useful in design of high speed and high density parallel adders and multipliers.

key words: *pass-transistor logic, carry skip method, booth multiplier, monte carlo method.*

1. Introduction

Upon the application of high-speed digital signal processing system on VLSI, various signal processors have been developed these years. Among those circuits, parallel multipliers are usually a core for hardware implementation of many arithmetic or graphics processing algorithms. Certainly, speed performance of these multipliers is very important in concerning performance of the whole systems. Besides conventional CMOS logics, CPL (Complementary Pass-transistor Logic) [2] and DPL (Double Pass-transistor Logic) [3] are solutions to such requirements. CMOS is not totally satisfactory when high speed performance is required. For CPL and DPL configuration, the layout area, including double wire routing space, are relatively bulky as compared to conventional CMOS circuits.

Recently, a logic synthesis scheme called LEAP was proposed for integration of pass-transistor logic [4]. Although some combinational circuits obtained from this scheme showed advantages over conventional CMOS circuits, comparison with dual-rail logics was not reported. In particular, the application of the LEAP scheme to design of systematic arithmetic logics (like parallel adders and multipliers) was not fully stated.

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Furthermore, the previous DPL and LEAP designs were done in CMOS processes with 3-metal layers. It is rather restrictive to general designers who use common channel routers or layout tools for simpler CMOS fabrication process.

In this paper, the use of regenerative elements in dual-rail logics for design of parallel adders and multipliers was investigated. In addition, a combination of single-rail and dual-rail signals, which is useful for 2-metal layer CMOS layout processes, with the employment of REGEN element is also proposed. Conceptually, RPL combines advantages of both the compact size of CPL and the full voltage-swing of DPL, and is featured by high operation speed, reasonable power consumption, and wide application [1]. The technique can be applied to basic logic gates, full adder, data compressors (e.g. 4-2 compressor), multiplier units, and more complicated arithmetic logics like Conditional Carry Select (CCS) circuit. The magnitude of propagation delay time of RPL is smaller than the conventional CMOS, CPL, DPL and LEAP. In previous work like [2], basic CPL gates were suggested but the AND2 and OR2 gates were not actually used in the design. In this work, however, usage of most basic gates is addressed. Low power consumption can also be achieved by reduced number of transistors and metal interconnections. Data on timing simulation and layout also proved that RPL is advantageous over existing dual-rail logics while considering speed, power consumption and layout area.

RPL can be viewed as a derivative of CPL [2], but it uses less number of transistor by replacing the level restoring inverters with cross-coupled pMOSFET pairs. Consider the RPL basic gates and the full adder in Fig. 1. These gates are featured by the short propagation delay time from all inputs to outputs (both true and complement). Among these gates, the full adder, FA, was proved to be a promising unit for high-speed and low-power logic design [1]. In addition, since the carry path (C to Co) of the FA is only of one pass-transistor delay, it is especially useful for applications like the Manchester carry chain, carry skip adders [5], and multiplier trees (Sect. 3.2).

2. Design of RPL Adders

It was concluded in previous work [1] that RPL full adder is the fastest one among the six representative full

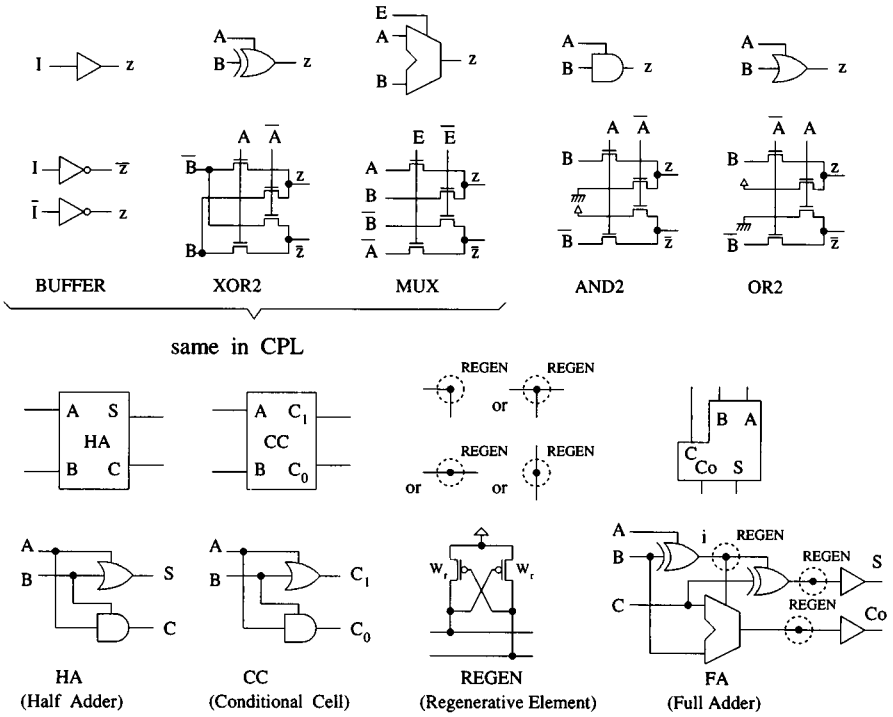


Fig. 1 Symbols and the corresponding RPL circuits.

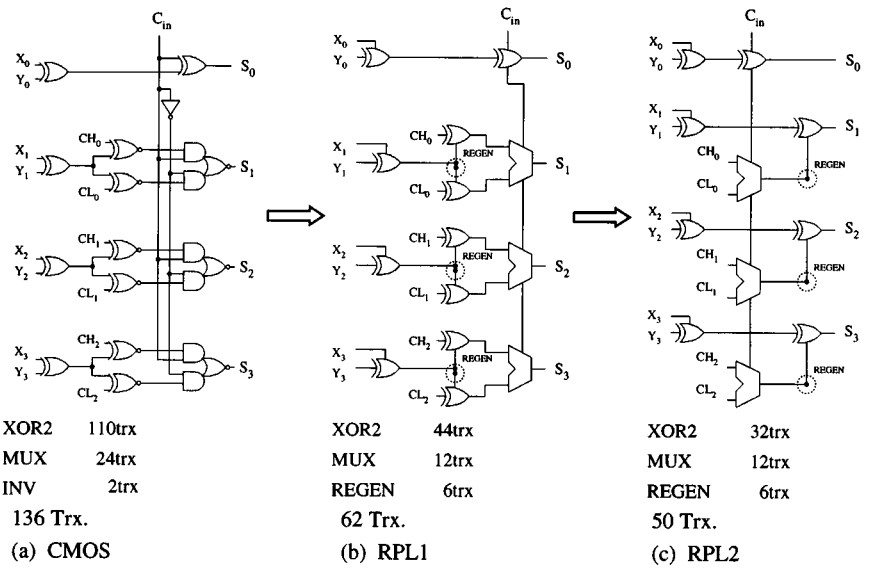


Fig. 2 Modification of the RPL Conditional Sum Select (CSS) circuits (4-bit): (a) CMOS, (b) RPL1, (c) RPL2.

adders (RPL, CPL, DPL, conventional CMOS, TG, and TSPC). Together with the basic RPL gates defined in Fig. 1, it was also concluded that one of the advantages of RPL is the building block structure for high-speed arithmetic logics like addition and multiplication. One of the examples is the Conditional Carry Select (CCS) circuit for addition logics[3]. This circuit is featured by short critical path delay and compact layout.

On the other hand, Conditional Sum Select (CSS) circuit is a logic circuit which computes the arithmetic sum according to a "carry-in" signal and a group of conditional carry signals. Modification of the RPL CSS circuit from conventional CMOS circuit is shown in Fig. 2. It is noted that the number of transistor was dramatically reduced (approximately half) when RPL circuits are used. RPL1 and RPL2 are two options of RPL implementation. RPL1 is a direct derivative from the CMOS configuration while RPL2 is a modification of RPL1 with less gate count but longer delay from node C_{in} to "S" outputs.

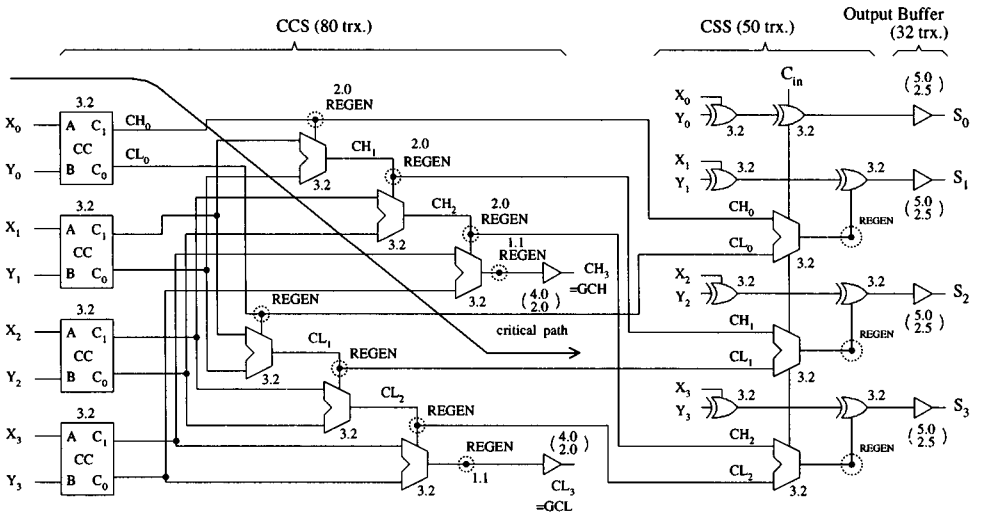


Fig. 3 The RPL Conditional Carry and Sum Select (CCSS) circuits (4-bit).

Table 1 Features of the FA, W4, CCS and CCSS circuits on DPL, RPL, conventional CMOS circuit configurations, and the LEAP system [4]; and data of 8×8, 12×12, 16×16 bit parallel multipliers.

Circuit	type	no. of trx.	layout area	worst case t_{pd} (ns)	Avg. Power (mW) at 330 MHz data rate
FA	DPL [3]	32	1292 μm^2	0.58	1.03
	CPL [2]	28	1370 μm^2	0.60	1.10
	RPL	22	780 μm^2	0.46	0.93
	CMOS [2]	40	2480 μm^2	0.62	1.05
	LEAP [4]	24	870 μm^2	0.52	0.90
W4 (4-2 compressor)	DPL	60	4280 μm^2	0.72	1.80
	RPL	50/[40]	2110/[1980] μm^2	0.68/[0.72]	1.12/[1.04]
	CMOS [11]	70	3950 μm^2	0.95	1.22
	LEAP	64	3670 μm^2	1.12	0.70
CCS	DPL	152	7296 μm^2	0.84	1.74
	RPL	80	4096 μm^2	0.79	1.35
	CMOS	96	4494 μm^2	1.25	0.95
	LEAP	86	4174 μm^2	1.95	0.95
CCSS	DPL	310	0.0320 mm^2	0.94	2.33
	RPL	162	0.0113 mm^2	0.85	1.85
	CMOS	200	0.0152 mm^2	1.45	1.35
	LEAP	170	0.0102 mm^2	2.15	1.35
8×8b multiplier	DPL	2900	0.375 mm^2	3.54	20.4
	RPL	1990	0.215 mm^2	2.75	18.8
	Sgl. RPL	1662	0.186 mm^2	2.79	16.5
	CMOS	2048	0.190 mm^2	3.75	13.0
12×12-b multiplier	Sgl. RPL	3620	0.4265 mm^2	3.99	34.0
	DPL	5900	0.7750 mm^2	4.34	40.0
16×16-b multiplier (3-metal layer)	Sgl. RPL	5200	0.9520 mm^2	4.50	84.0
	CPL [2]	8500	2.0300 mm^2	5.20	140.0

N.B. 1. Values in [ ] bracket indicates data of basic RPL circuit.
2. t_{pd} was measured at 50% to 50% transition of input and output signals.
3. Unless otherwise stated, circuits were designed on 2-metal layer process.

Number of transistors of the CSS circuit is reduced from 136 in CMOS to 50 in RPL2. Usually, it is costly to implement carry select adders in conventional CMOS gates because there is a number of XOR and MUX gates, which are composed of 10 and 8 transistors respectively, in an adder. As a result, the transistor count is nearly doubled in CMOS circuits. In RPL, however, the configuration becomes very simple (for instance, as the circuit shown in Fig. 2). Such arrangement reduces three XOR2 gates but increase one gate delay in the critical path. Such compensation is reasonable when the whole performance of the adder (or multiplier) is considered. Guidelines of determination of the transistor widths can be found in [1].

Then, the CCS circuit in [3] and the CSS circuit stated in Fig. 2 can be combined to form the Condi-

tional Carry and Sum Select (CCSS) circuit (Fig. 3), which is applicable to addition circuit, for design of parallel adders. Detailed transistor widths are indicated beside each gates for reader's interest. Data of timing and layout area of this circuit as compared with CMOS, DPL and LEAP circuits are summarized in Table 1.

Simulation was done with Spice3e on SunSparc workstation with standard 0.5 μm process parameters. The supply voltage is 3.0 V; the threshold voltages of nMOSFETs and pMOSFETs are 0.5 V and -0.5 V respectively; and the transconductance coefficients of nMOSFETs and pMOSFETs are $60\mu A/V^2$ and $30\mu A/V^2$, respectively. All placement and routing were done with a semi-automatic layout system called MOSES (MOS circuit Synthesis and Evaluation System), with adjustable automatic cell placement and manual routing. Here, 2-metal layer process is used to illustrate implementation on simpler fabrication process.

It is also noted that the total number of transistors in the RPL CCSS circuit is not as advantageous as that in the CSS portion, as stated above. It is because there is certain number of transistors in dual-rail output buffers and the "CCS" circuit which is part of the whole CCSS adder. This point can be improved if outputs of the CCSS circuit are connected directly to output drivers or pads.

3. Design of Multipliers

The multiplier consists of Booth decoders, array(s) of partial product (PP) generators, a parallel multiplier tree structured with Booth algorithm and a final adder (Fig. 4 (a)). The structure of multiplier tree in higher or-

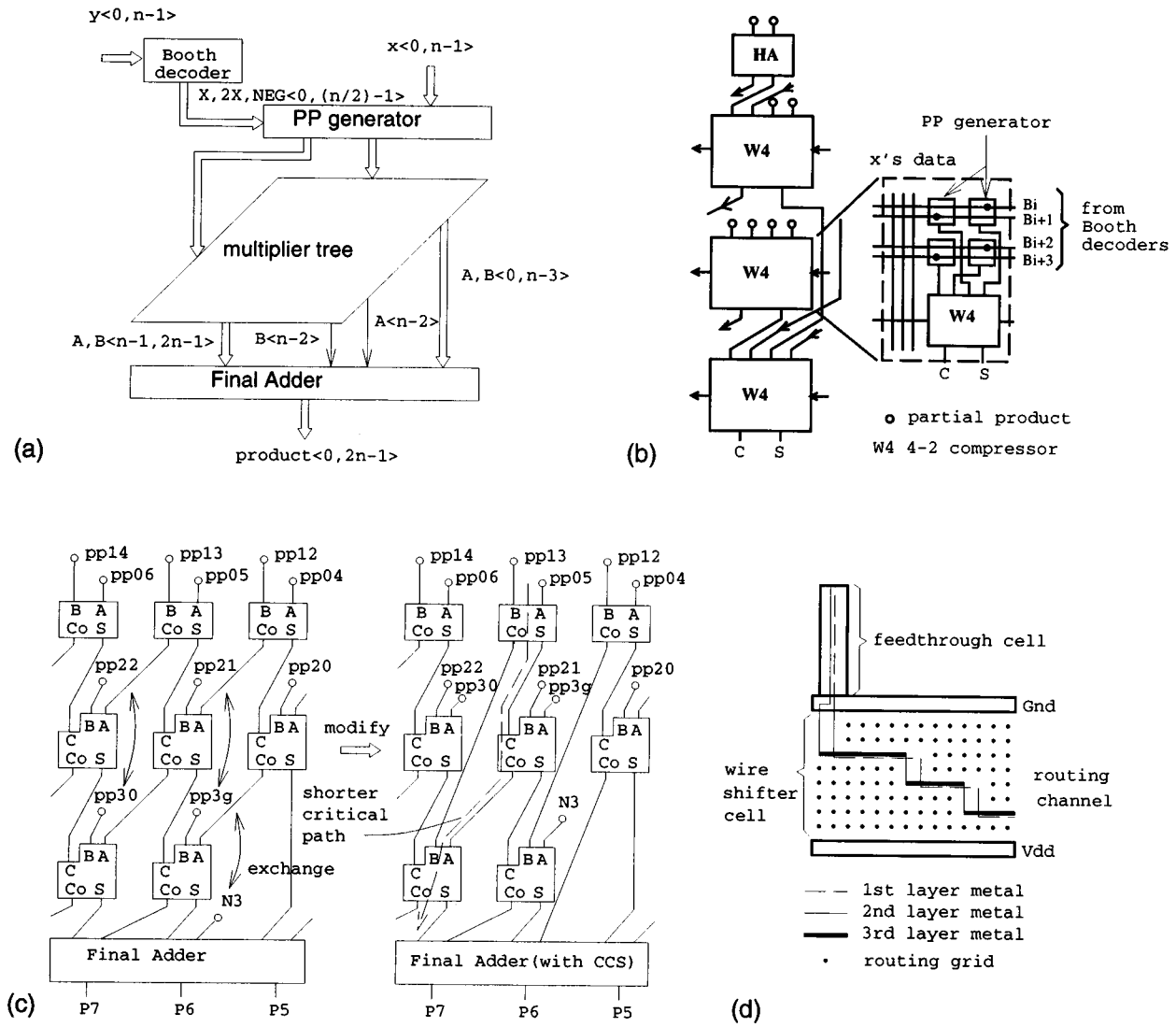


Fig. 4 (a) Block diagram of an n×n bit Booth multiplier, (b) Part of multiplier tree and cell structure of a 16×16 bit Booth multiplier (w4 denotes 4-2 compressor), (c) Modification from Carry Save Array (CSaveA) to Carry Skip Array (CSkipA) in the multiplier tree in an 8×8 bit Booth multiplier, and (d) Wire connection strategy in 3-metal layer process.

der multipliers prefers usage of 4-2 compressors (W4 in Fig. 4 (b)), as that in a 16×16 bit multiplier (Fig. 4 (b)). While in multipliers of small scale, the options may be as those shown in Fig. 4 (c) [6].

3.1 Design of Booth Decoder and Partial Product (PP) Generator

In designing large scale multipliers, layout area is one of the most important points to be considered. One of the disadvantages of dual-rail (complementary) logic is the redundancy of double routing area. As shown in Fig. 5, which corresponds to the floorplan of 16×16 bit Booth multipliers (3 metal layer process), wire shifter cells are used to reduce design time of wiring [7]. It is noted the horizontal distance within the wire shifter cells is the main portion (length), as compared to the vertical one. As a result, a wire connection strategy for 3 metal layer process is proposed to deal with this phenomenon. As shown in Fig. 4 (d), the dual-rail signals run on the first and the third metal layers in the horizontal direction, and turn to run on the second metal layer in the vertical direction. Then, the dual-rail signals occupy only one routing channel in the horizontal direction, while allowing horizontal wires of other dual-rail signals pass effectively. Similarly, vertical connection inside the feedthrough cells uses the first and the second metal layers. This method greatly reduced routing complexity as well as layout area.

Since the Modified Booth's algorithm is widely used in the design of multiplier, the Booth decoder and PP generator (which RPL implementation is shown in Fig. 6 (a)) are constructed. This decode system belongs to the radix-2 multiplication scheme of the Modified Booth's algorithm [5]. A multiplicand, either x_j or x_{j-1}, is selected depending on whether decoded data, X or 2X is high and inverted by the decoded data NEG [8]. Since the number of PP generators is usually large in a multiplier (128 in a 16×16 bit Booth multiplier, and 512 in a 32×32 one), it is important to reduce the size of a PP generator cell. To tackle the problem, circuitry of the partial product generator is modified as in Fig. 6 (b). It is noted that the circuit is rather simple due to use of single-rail pass-transistors and the introduction of "don't care" condition. (According to the Modified Booth's Algorithm [5], the signals X and 2X never appear to be "1" at the same time.)

As a result, the partial product generator is simpli-

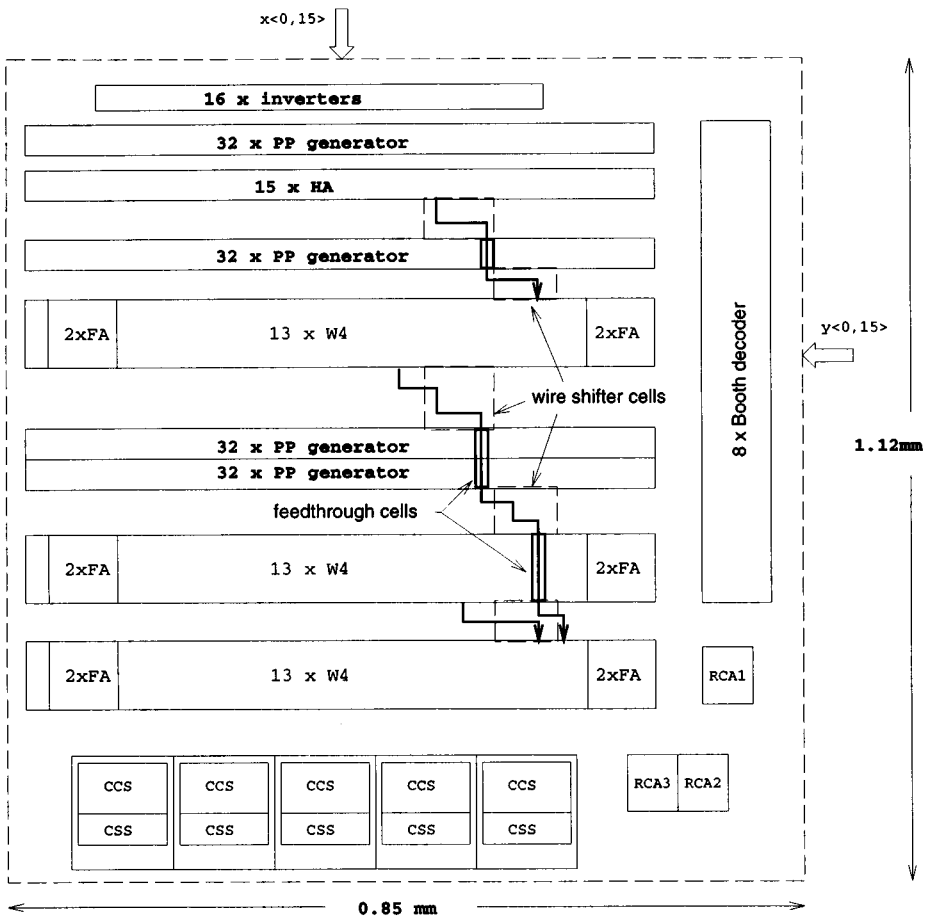
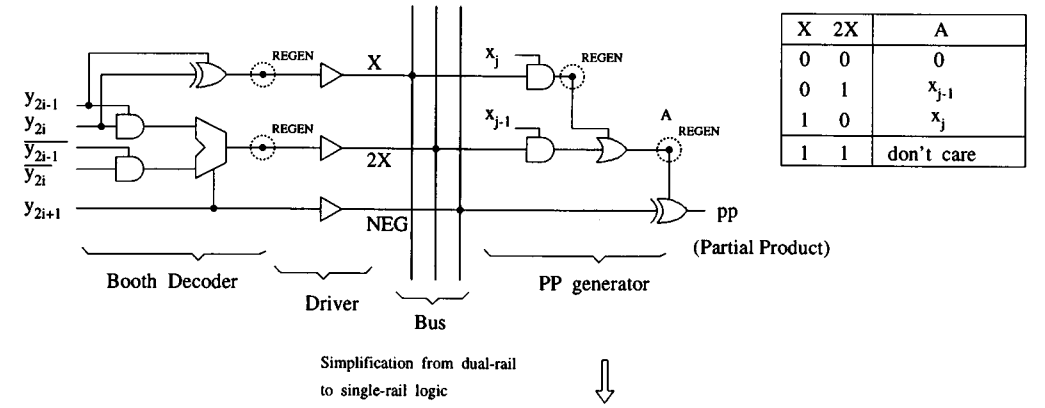
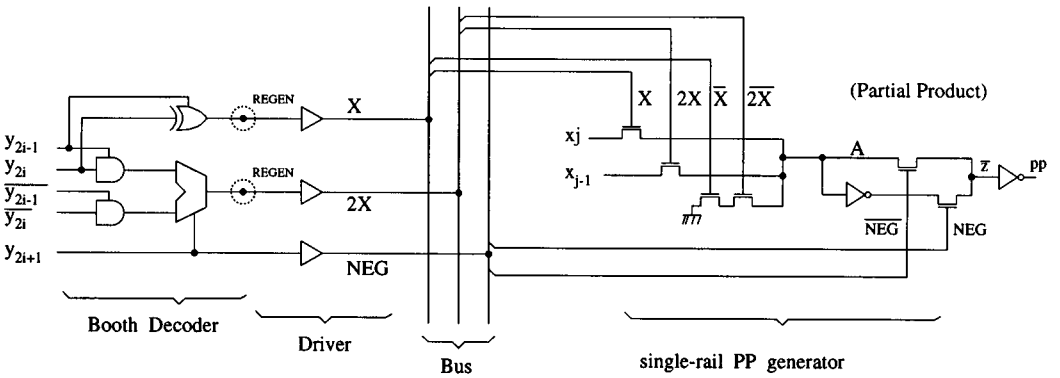


Fig. 5 Floorplans of the RPL 16×16 bit Booth multiplier (3 metal layer process).



X	2X	A
0	0	0
0	1	x_{j-1}
1	0	x_j
1	1	don't care

(a) Dual-rail partial product generator



(b) Single-rail partial product generator

Fig. 6 Booth Decoder and Partial Product Generator: (a) Dual-rail implementation, (b) Single-rail implementation.

fied to save routing area. Comparison of layout area is summarized on the result of the 8×8 bit RPL Booth multipliers in Table 1. The simulation conditions are the same as those of the adder design (Sect. 2). It is concluded that the single-rail RPL implementation can reduce layout area with little compensation in critical path delay.

An analysis of the effect of signal skew in CPL and RPL circuit is illustrated in Fig. 7. With different conditions on circuit parameters, it is concluded that the signal skew in RPL circuit is smaller than those in CPL circuit, even if input signals to the nMOS pass-transistor gate are delayed or distorted after transmission through a long connection wire. As a result, another feature of the REGEN element is its inherent capability to reshape "reproduced" dual-rail signals after a long single-rail transmission and applies to high-speed logic portion. (The longest wire length, 200 μm, inside the 12×12 bit multiplier is highlighted in the graph for reference.) In other words, REGEN element can make complementary signal skew smaller even if the waveform of the input signals into the nMOS pass-transistor circuit degrades. Upon the test on signal skew of various basic gates with Monte Carlo method, it is found that the maximum skew in RPL is 50 ps while that in CPL is 85 ps.

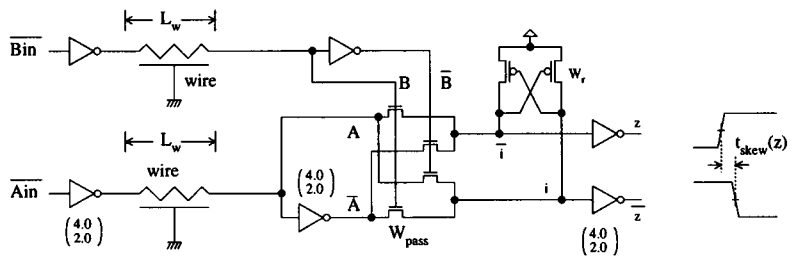
While considering settings of threshold voltages of the buffering inverters, the following equation [5] is used:

$$V_{th} = \frac{\sqrt{K}(V_{dd} - |V_{Tp}|) + V_{Tn}}{1 + \sqrt{K}} \tag{1}$$

where

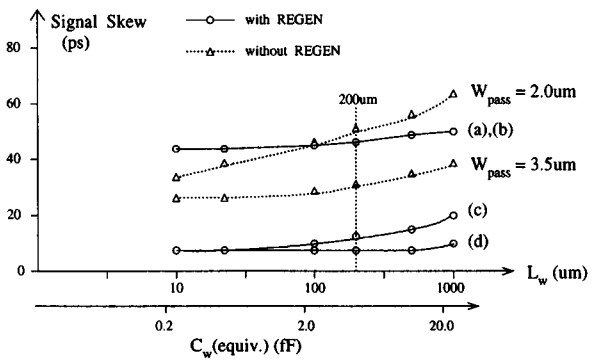
$$K = \frac{\beta_p}{\beta_n} = \frac{\mu_p W_p}{\mu_n W_n} \cong \frac{W_p}{2W_n}.$$

Without REGEN elements, the threshold voltage of the buffering inverters should be set at about $(V_{dd} - V_{Tn})/2$ for better noise margin in circuit. Hence, value of (W_p/W_n) would be around 0.7 to 0.8, and it is difficult to obtain balanced driving force because of the weak mobility of the pMOSFET. Such unbalanced driving forces of the nMOSFET and pMOSFET of the inverter would result in unbalanced rise and fall time of the output signals. Hence, there is relatively large signal skew in the "true" and "complement" signals of a CPL circuit.



(a)

Condition	W_{pass}(um)	W_r (um)
a	2.4	0.8
b	3.5	0.8
c	2.4	2.0
d	3.5	2.0



(b)

Fig. 7 Signal skew behaviour in RPL circuits: (a) XOR2 gate test set, (b) signal skew time versus length of metal interconnection, with and without REGEN element.

3.2 Design of the Multiplier Tree

Figure 4(c) shows the well-known structure of a parallel array multiplier in an 8×8 bit Booth multiplier. Using a carry-save adder (CSA) technique for the multiplier tree, it is readily observed that the data flow is vertical from one row to the next (where pp(ij) indicates the i, j-th partial product). Using the RPL full adder cell in Fig. 1, the critical path can be reduced by exchanging the 2 connections of partial products as shown in Fig. 4(c). This method is usually termed as Carry Skip Method [1], [6], and is especially useful in designing multiplier with small length (e.g. 8×8 bit or 12×12 bit).

In those advanced multipliers with higher order counters or compressors, horizontal connection through "carry-in" and "carry-out" signals simplify connection and shorten delay on the vertical direction (Fig. 4(b)) [3], [9]. In Fig. 4(b), Bi denotes the combined bus of X_i, $2X_i$ and NEG_i. Use of 4-2 compressors in the multiplier tree was proved to be able to reduce delay time and power consumption [3], [10]. Using RPL configuration, the 4-2 compressor as shown in Fig. 8 was obtained. Using basic RPL and higher speed RPL, sizes of the compressor are solely 40 and 50, respectively. Such circuit are smaller and faster (Tables 1 and 2) than conventional circuits [10], [11].

Design procedure of the 4-2 compressor is illustrated with steps as ordered in Figs. 8(a)–(c). Similar to traditional logical optimization methods, the final circuits are generated by merging the common nodes in the partial functional modules. In this example, nodes m and n are merged to obtain the final cirucit configuration. Other gates or modules (e.g. 6-2 and 7-3 compressors) can also be synthesized by similar procedure.

Table 2 Comparison of transistor count of modules in the parallel multipliers with various circuit configurations.

	CMOS	CPL	DPL	LEAP	RPL
Booth Decoder	38	36	48	30	36
PP Generator	18	28	32	14	10
FA	24	28	32	24	22
HA	14	12	16	14	8
4-2 compressor	70	54	60	64	50/[40]

N.B. Value in [ ] bracket indicates number of transistor in basic RPL circuit.

3.3 Design of the Final Adder

Since the least and most significant product bits of the input to the final adder arrive first, while the bits between arrive later, a type of adaptive final adder was proposed by Oklobdzija [9]. Such final adder is characterized by proper combination of adder portion to save layout area and energy resource. In this work, this method is employed in design of the final adder.

Refer to the signal arrival profile of the multiplier trees of the 8×8 bit and 16×16 bit multipliers (Fig. 9), the final adder is divided into several portions in term of "the slope of delay time with respect to the product bit position" ("slope" in short). They are (i) ripple carry adders (RCA) for the positive slope region, and (ii) conditional carry and sum select (CCSS) modules (Fig. 3) for the flat top and the negative slope region. In the

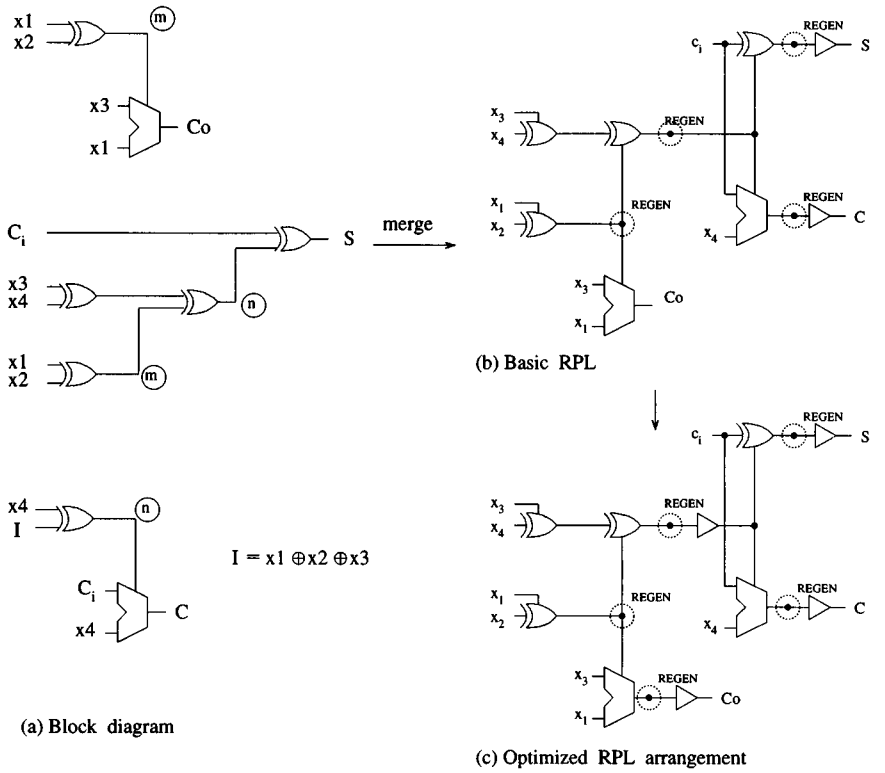


Fig. 8 Design procedure of the RPL 4-2 compressor: (a) Block diagram, (b) Basic RPL, (c) Optimized RPL arrangement.

portion of the final adder of the 16×16 bit multiplier, three ripple carry adders (RCA1, RCA2 and RCA3) was used for the first 12-bit to save resource, i.e. power consumption and layout area. The "carry in" signal to RCA2 is generated from a carry lookahead circuit from RCA1. Similarly, "carry in" signal to RCA3 is generated from RCA2. The CCSS adder is chosen for the portion at flat top and negative slope region because of its high performance, small number of transistor count, and compact layout with the implementation of RPL.

A comparison of the simulation results of RPL circuits with those of conventional CMOS, DPL and the LEAP system is summarized in Table 1. Transistor count of mostly related logic families are concluded in Table 2.

4. Results and Discussion

The RPL FA shown in Fig. 1 is used for design of the multiplier trees of 8×8 bit and 12×12 bit parallel multipliers. The propagation delay from A/B and C to S/Co are 0.42 ns and 0.25 ns, respectively, according to the same conditions as stated in Sect. 2. Because of the short delay path from C to Co, it facilitates application of the carry skip method in the multiplier trees. As compared with major full adders (conventional CMOS, CPL, DPL, and pass-transistor logic from the LEAP system), the RPL full adder can achieve the highest clock frequency while attaining a reasonably low power consumption among dual-rail logics. By investigation on the simulation results, it is found that RPL performs better than other dual-rail pass-transistor logics (CPL and DPL) because it consists of less number of transistors and requires less metal interconnections. For the same reason, power consumption is also small among these dual-rail pass-transistor logics.

Considering the propagation delay time and layout area of the multipliers with single-rail and dual-rail PP generator, it is concluded that there is only a little compensation (less than 2 percents) on the delay time and a certain amount in reduction of the layout area (larger than 15 percents) in the 8×8 bit mutliplier. As shown in Fig. 10, it is found that layout area of wiring in RPL circuit is larger than that in conventional CMOS circuit, although area of RPL's logic cells is smaller. With proper combination of single-rail and dual-rail signals, it is possible to obtain a high-speed and high-density multiplier circuit with the modified (or generalized) RPL methodology. (1) Comparison of the FA, 4-2 compressor, CCS and CCSS circuits by DPL, RPL, CMOS and LEAP circuits; (2) comparison of the 8×8 bit parallel multipliers by DPL, RPL and CMOS; and (3) the RPL 12×12 bit parallel multiplier (with single-rail dual-rail conversion) are summarized in Table 1. It is noted that RPL is featured by compact layout area and shorter critical path delay in these circuits. It is

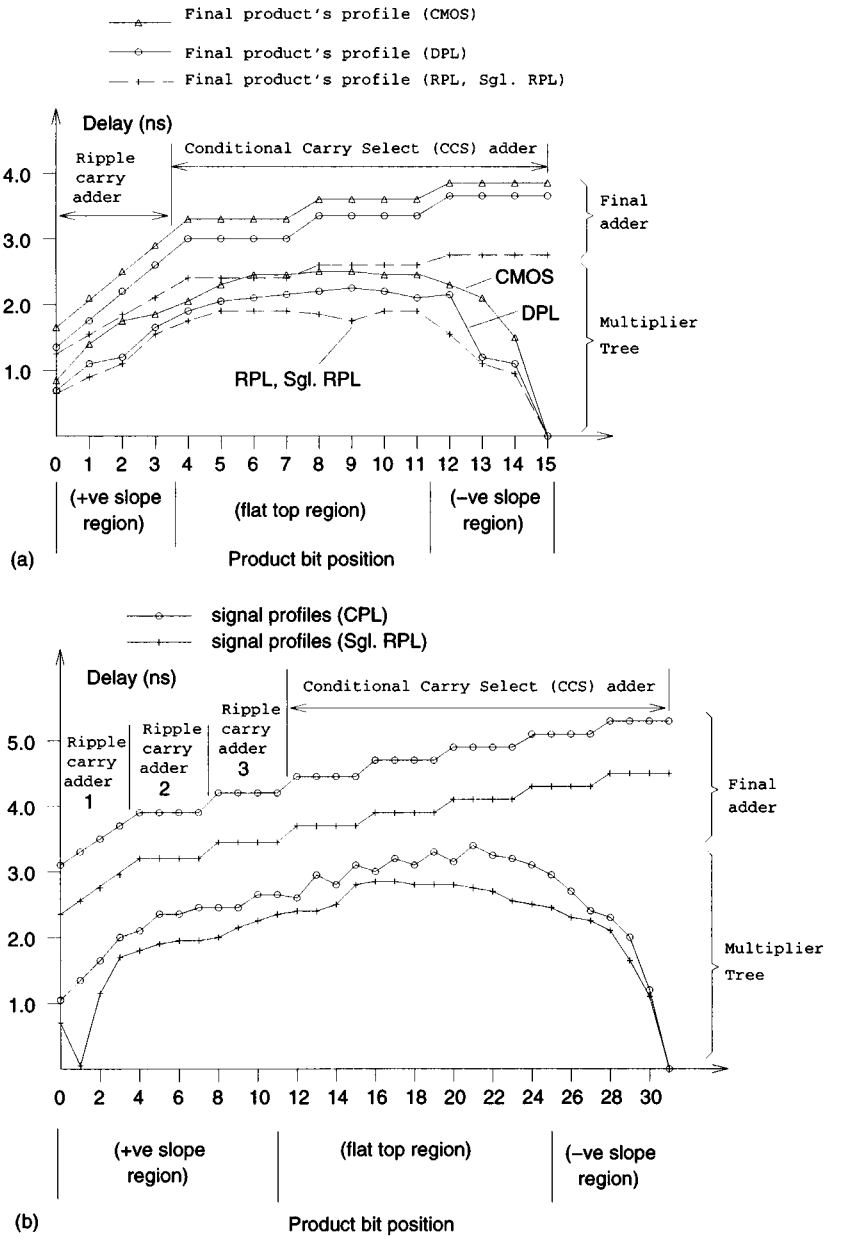


Fig. 9 Signal arrival profiles from the multiplier trees and the final adders of the Booth multipliers: (a) 8×8 bit, (b) 16×16 bit (Sgl. RPL: RPL with single-rail dual-rail signal conversion).

also concluded that LEAP can generate low power circuits. But, RPL shows advantages in obtaining shorter critical path delay in these example circuits.

Although the numbers of transistors in RPL circuits is smaller than those in CMOS circuits, their layout area cannot be smaller than those of CMOS circuits. The main reason is that there is extra routing area in the RPL circuits as 2-metal layer process is used.

While designing multipliers of higher orders, it is suggested to use 4-2 compressors or data compressors of high orders for better regularity of layout and more structural design. A 16×16 bit Booth multiplier is used as example to evaluate the performance of RPL circuit, while that of CPL is used for comparison. In addition, 3-metal layer process is used for design of these multipliers because there is large amount of long dual-rail signal connection.

In this work, optimization of size of transistors in the circuits was achieved by a two-step optimization method including Monte Carlo method. In the first step, Monte Carlo method with independent random variables on W were chosen for each circuit, where W is the value of transistor gate width. The minimum and maximum transistor width, W, were set to 0.8 μm and

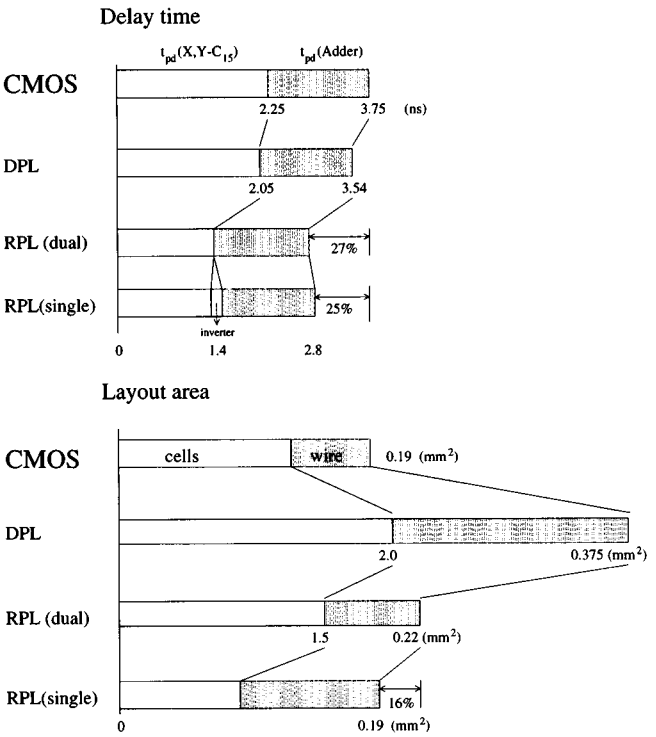


Fig. 10 Propagation delay and layout area of the 8×8 bit Booth multiplier with conventional CMOS, DPL and RPL (with dual-rail and single-rail PP generators).

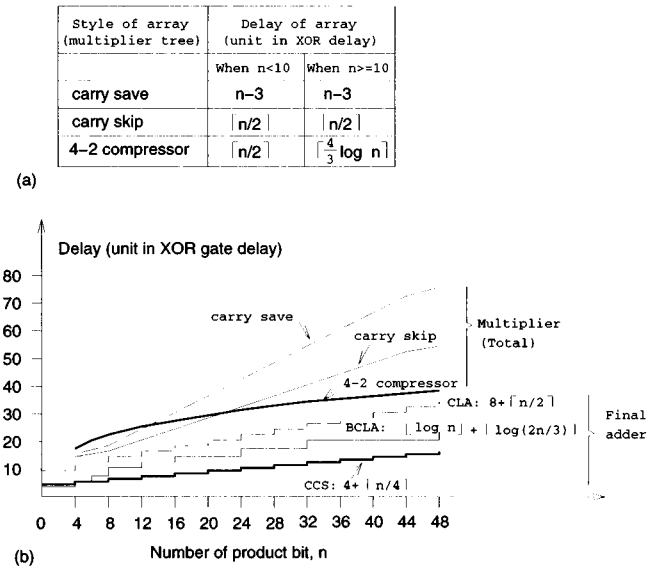


Fig. 11 (a) Features of RPL multipliers with different architectures, (b) Order of propagation delay versus size of multipliers. $\lfloor x \rfloor$ and $\lceil x \rceil$ are the maximum integers less or equal to x and less than $x+1$, respectively. (All logarithmic functions are with base 2.)

5.0 μm, respectively. And, in the second step, exhaustive search method with range of variation of W within $\pm 0.5\,\mu$m and step of variation at 0.1 μm was done. Such optimization method confirms that circuits under comparison were set to their most favourable conditions [1].

For the same reason, Monte Carlo simulation method for power estimation was done for a finite set of independent test patterns (including critical path test patterns) to obtain a reasonably accurate estimation of the power consumption of the whole circuit under comparison [12].

A preliminary prediction of the performance of RPL parallel multipliers is made and the data are plotted on the graph of Figs. 11 (a) and (b). When considering structure and performance of the multiplier tree (or array), it is noted that Carry Skip Method is superior in multiplier with shorter bit length (with n less than 10). When considering design of adders, it is found that CCS is faster than conventional CLA (Carry Lookahead Adder) and BCLA (Binary CLA) within a wide range of bit number (from 4 bit to 48 bit). In terms of routability, Carry Skip Method is is facilitated by its simple structure and compactness of the full adder (FA) cell. Here, the combination of single-rail and dual-rail routing discussed above will release the problem of huge routing capacity in wide multipliers to some extent as far as signal skew on the regenerated dual-rail signals is endurable. Certainly, increased number of metal layers will be a solution to the routing problem. In this work, the 2-metal layer process is used for smaller designs to show the possibility of implementation of frequently used arithmetic logic with more common layout process. On the other hand, 3-metal layer process with systematic routing strategy is used to design more complicated system for higher efficiency during layout.

5. Conclusion

Design of parallel adders and multipliers using a modular dual-rail circuit design methodology, Regenerative Pass-transistor Logic (RPL), was introduced. Several circuit modules, 8×8 bit and 12×12 bit parallel multipliers designed with standard 2-metal layer CMOS layout process were used as examples to illustrate the general functionality of RPL. And, a 16×16 bit Booth multiplier is designed for evaluation of RPL's potential in larger arithmetic system. RPL shows advantages over other dual-rail pass-transistor logics, such as CPL or DPL, while concerning transistor count, input capacitances, and metal interconnections. As compared to the pass-transistor logic synthesis scheme, LEAP, RPL shows advantages in obtaining shorter critical path delay in certain number of example circuits, although LEAP can generate low power circuits. And, carry skip method is employed in the multipliers to achieve shorter critical delay. Moreover, a single-rail to dual-rail signal connection technique using REGEN element is also proposed for high-speed high-density multiplier designs. RPL is also proved to be stronger than CPL on signal skew reduction. Simulation results on CCS adders and

the parallel multipliers also confirm that RPL performs well in terms of propagation delay, power consumption and layout area.

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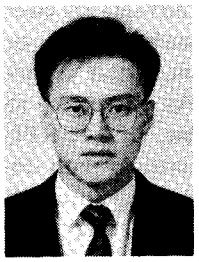

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