

SPECIFICATIONS

PCI-DAS08

Analog Inputs + DIO + Counters



**MEASUREMENT
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Typical specifications for 25 DegC unless otherwise specified.

Power consumption

+5V Operating (A/D converting to FIFO)	251 mA typical, 436 mA max
+12V	13 mA typical, 19 mA max
-12V	17 mA typical, 23 mA max

Analog input section

A/D converter type	AD1674J
Resolution	12 bits
Ranges	±5V
A/D pacing	Software polled

A/D Triggering Modes	
Digital	Software polling of digital input followed by pacer loading and configuration.

Data transfer	Software polled
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Polarity	Bipolar
Number of channels	8 single-ended

A/D conversion time	10 μs
Throughput	40KHz typical, PC dependent

Relative Accuracy	±1LSB
Differential Linearity error	No Missing Codes guaranteed
Integral Linearity error	±1 LSB
No missing codes guaranteed	12 bits

Gain drift (A/D specs)	±180ppm/°C
Zero drift (A/D specs)	±60ppm/°C

Input leakage current	±60 nA max over temperature
Input impedance	10Meg Ohms min
Absolute maximum input voltage	±35V

Noise Distribution (Rate = 1-50KHz, Average % ±2 bins, Average % ±1 bin, Average # bins)

Bipolar (5V)	100% / 100% / 3 bins
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Digital Input / Output

Digital Type (Main connector)	
Output	74ACT273
Input	74LS244
Configuration	3 fixed input, 4 fixed output
Number of channels	7
Output High	3.94 volts min @ -24mA (V _{cc} = 4.5V)
Output Low	0.36 volts max @ 24mA (V _{cc} = 4.5V)
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min
Interrupts	INTA# - mapped to IRQ _n via PCI BIOS at boot-time
Interrupt enable	Programmable through PCI controller; 0 = disabled, 1 = enabled (default)
Interrupt sources	External source (EXT INT), polarity programmable through PCI controller; 1 = active high, 0 = active low (default)

Counter section

Counter type	82C54
Configuration	82C54 device. 3 down counters per 82C54, 16 bits each
	82C54:
	Counter 0 - User Counter 1
	Source: Available at user connector (CTR1CLK)
	Gate: Available at user connector (CTR1GATE)
	Output: Available at user connector (CTR1OUT)
	Counter 1 - User Counter 2
	Source: Available at user connector (CTR2CLK)
	Gate: Available at user connector (CTR2GATE)
	Output: Available at user connector (CTR2OUT)
	Counter 2 - User Counter 3 or Interrupt Pacer
	Source: Buffered PCI Clock (33MHz) divided by 8.
	Gate: Available at user connector (CTR3GATE)
	Output: Available at user connector (CTR3OUT) and may be software configured as Interrupt Pacer.
Clock input frequency	10Mhz max
High pulse width (clock input)	30ns min
Low pulse width (clock input)	50ns min
Gate width high	50ns min

Gate width low	50ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental

Operating temperature range	0 to 50 °C
Storage temperature range	-20 to 70 °C
Humidity	0 to 90% non-condensing

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