ANEXOS

7. ANEXOS

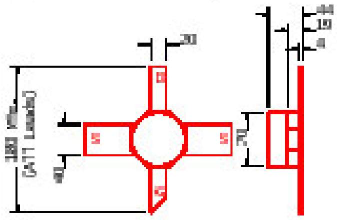
7.1. HOJA DE CATÁLOGO DEL TRANSISTOR EPBO18A5-70

Excelics **EPB018A5/A7/A9-70**

DATA SHEET

Super Low Noise High Gain Heterojunction FET

- NON-HERMETIC LOW COST CERAMIC 70 mil PACKAGE
- TYPICAL 0.50~0.90dB NOISE FIGURE AND 11.5~13.0dB ASSOCIATED GAIN AT 12GHz
- 0.3 X 180 MICRON RECESSED " MUSHROOM" GATE
- Si_3N_4 PASSIVATION
- ADVANCED EPITAXIAL HETEROJUNCTION PROFILE PROVIDES SUPER LOW NOISE, HIGH GAIN AND HIGH RELIABILITY



All Dimensions In mils.

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOLS	PARAMETERS/TEST CONDITIONS		MIN	TYP	MAX	UNIT
NF	Noise Figure, f=12GHz Vds=2V, Ids=15mA	EPB018A5-70		0.50	0.60	dB
		EPB018A7-70		0.65	0.80	
		EPB018A9-70		0.95	1.20	
Ga	Associated Gain, f=12GHz Vds=2V, Ids=15mA	EPB018A5-70	11.5	13.0		dB
		EPB018A7-70	11.0	12.5		
		EPB018A9-70	10.5	11.5		
P_{1dB}	Output Power at 1dB Compression Vds=3V, Ids=25mA	f=12GHz f=18GHz		15.0 15.0		dBm
G_{1dB}	Gain at 1dB Compression Vds=3V, Ids=25mA	f=12GHz f=18GHz		14.0 11.5		dB
Idss	Saturated Drain Current Vds=2V, Vgs=0V		15	45	80	mA
Gm	Transconductance Vds=2V, Vgs=0V		50	90		mS
Vp	Pinch-off Voltage Vds=2V, Ids=1.0mA			-0.8	-2.5	V
BVgd	Drain Breakdown Voltage Igd=10uA		-3	-6		V
BVgs	Source Breakdown Voltage Igs=10uA		-3	-6		V
Rth	Thermal Resistance			480*		°C/W

*Overall Rth depends on case mounting.

MAXIMUM RATINGS AT 25°C

SYMBOLS	PARAMETERS	ABSOLUTE[1]	CONTINUOUS[2]
Vds	Drain-Source Voltage	5V	4V
Vgs	Gate-Source Voltage	-3V	-2V
Ids	Drain Current	Idss	60mA
Igsf	Forward Gate Current	2mA	0.3mA
Pin	Input Power	12dBm	@1dB Compression
Tch	Channel Temperature	175°C	150°C
Tstg	Storage Temperature	-65/175°C	-65/150°C
Pt	Total Power Dissipation	285mW	240mW

Note: 1. Exceeding any of the above ratings may result in permanent damage.
2. Exceeding any of the above ratings may reduce MTTF below design goals.

Excelics Semiconductor, Inc., 2908 Scott Blvd., Santa Clara, CA 95054
Phone: (408) 970-8664 Fax: (408) 970-8998 Web Site: www.excelics.com

EPB018A5/A7/A9-70

DATA SHEET

Super Low Noise High Gain Heterojunction FET

EPB018A5-70

S-PARAMETERS

2V, 15mA

FREQ	-- S11 --		-- S21 --		-- S12 --		-- S22 --	
(GHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.0	0.983	-18.6	6.245	162.2	0.019	78.9	0.530	-13.5
2.0	0.944	-37.5	5.964	144.3	0.036	65.2	0.507	-28.8
3.0	0.896	-55.5	5.582	127.7	0.050	53.6	0.485	-42.6
4.0	0.849	-72.6	5.327	112.4	0.063	43.6	0.464	-54.2
5.0	0.797	-89.2	5.111	97.6	0.074	33.1	0.421	-65.4
6.0	0.747	-103.7	4.799	83.4	0.081	23.4	0.370	-78.6
7.0	0.691	-118.6	4.503	69.9	0.085	13.9	0.344	-90.7
8.0	0.642	-132.8	4.277	57.0	0.088	4.7	0.303	-100.7
9.0	0.600	-155.6	4.189	42.7	0.093	-5.1	0.271	-111.2
10.0	0.567	-178.3	4.012	27.8	0.096	-16.3	0.228	-126.9
11.0	0.534	170.3	3.846	15.5	0.094	-26.5	0.193	-145.5
12.0	0.515	155.6	3.758	2.9	0.093	-33.1	0.177	-161.2
13.0	0.555	128.7	3.569	-12.5	0.091	-44.2	0.137	176.3
14.0	0.596	106.0	3.317	-27.1	0.088	-55.6	0.114	151.4
15.0	0.592	91.3	3.214	-41.3	0.087	-66.9	0.141	123.9
16.0	0.597	74.3	3.086	-56.8	0.083	-81.1	0.158	94.5
17.0	0.619	59.2	2.756	-69.5	0.071	-90.3	0.134	68.1
18.0	0.670	49.9	2.668	-79.4	0.071	-97.3	0.136	64.0
19.0	0.668	33.0	2.623	-95.4	0.069	-115.9	0.169	51.0
20.0	0.708	17.3	2.551	-111.1	0.064	-131.4	0.172	37.8
21.0	0.757	8.2	2.447	-125.1	0.061	-144.1	0.159	18.7
22.0	0.743	-2.5	2.325	-139.4	0.063	-159.2	0.135	14.7
23.0	0.726	-21.1	2.224	-158.5	0.065	179.4	0.115	-1.3
24.0	0.747	-39.6	2.063	-178.1	0.067	158.8	0.102	-39.6
25.0	0.709	-52.6	2.024	167.9	0.072	144.7	0.136	-56.6
26.0	0.683	-70.6	2.006	150.2	0.083	132.8	0.117	-71.3

EPB018A7-70

S-PARAMETERS

2V, 15mA

FREQ	-- S11 --		-- S21 --		-- S12 --		-- S22 --	
(GHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.0	0.985	-18.9	5.754	162.0	0.021	77.1	0.677	-13.7
2.0	0.949	-38.2	5.495	143.9	0.040	63.1	0.650	-28.9
3.0	0.903	-56.2	5.137	127.2	0.055	50.5	0.622	-42.7
4.0	0.860	-73.6	4.914	111.8	0.067	39.1	0.595	-54.1
5.0	0.812	-90.4	4.726	96.9	0.079	28.5	0.549	-65.4
6.0	0.765	-104.9	4.461	82.4	0.086	17.8	0.495	-78.6
7.0	0.713	-119.9	4.189	68.6	0.092	7.3	0.464	-90.5
8.0	0.664	-134.3	3.982	55.4	0.093	-3.6	0.411	-100.6
9.0	0.621	-157.1	3.908	40.9	0.096	-12.9	0.374	-108.6
10.0	0.591	-179.4	3.759	25.7	0.098	-24.5	0.328	-121.7
11.0	0.564	169.0	3.644	12.8	0.099	-33.4	0.295	-140.0
12.0	0.541	153.2	3.551	-0.8	0.098	-43.3	0.266	-157.6
13.0	0.574	126.2	3.360	-16.6	0.096	-54.9	0.210	-174.2
14.0	0.609	103.6	3.093	-31.7	0.090	-66.7	0.173	167.6
15.0	0.598	88.8	2.985	-46.4	0.090	-78.4	0.187	139.8
16.0	0.597	71.4	2.857	-62.2	0.085	-92.9	0.194	109.8
17.0	0.612	55.7	2.548	-75.5	0.072	-102.8	0.155	89.8
18.0	0.661	46.6	2.472	-85.8	0.076	-105.2	0.183	89.7
19.0	0.657	29.0	2.381	-102.1	0.076	-126.2	0.221	68.8
20.0	0.697	13.2	2.286	-118.1	0.071	-141.6	0.240	56.1
21.0	0.740	4.4	2.173	-131.8	0.068	-155.3	0.221	40.9
22.0	0.728	-5.8	2.067	-145.9	0.070	-167.9	0.210	36.8
23.0	0.717	-24.4	1.958	-164.5	0.071	172.5	0.188	21.8
24.0	0.743	-41.8	1.807	176.3	0.071	151.8	0.154	-5.5
25.0	0.710	-53.5	1.757	161.7	0.075	138.3	0.174	-28.1
26.0	0.689	-69.1	1.759	145.4	0.084	124.1	0.152	-47.5

EPB018A7-70

Noise Parameters

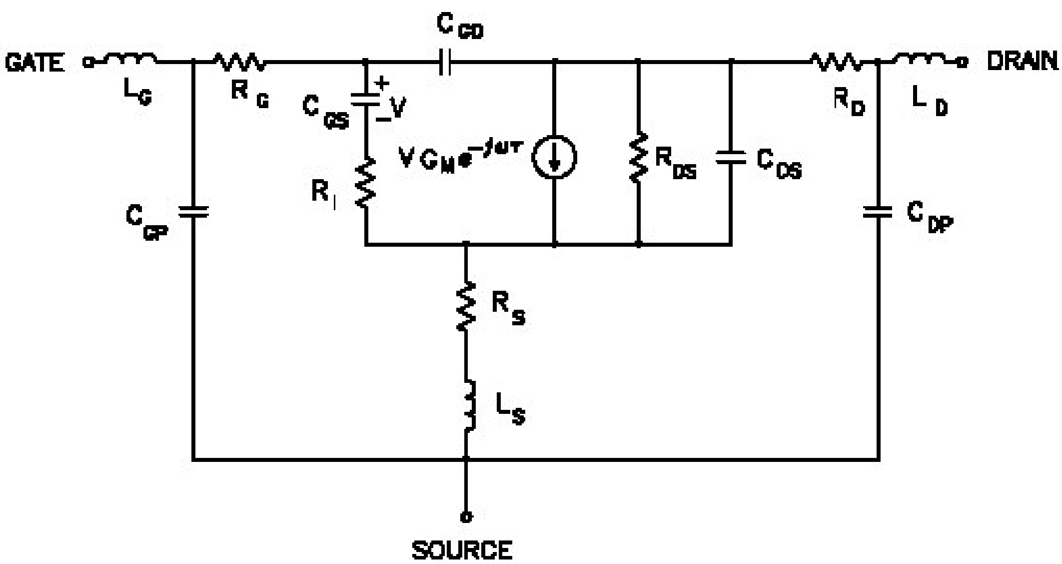
Vds=2V, Ids=15mA

Freq.	Gamma Opt		Nfmin	
(GHz)	(MAG)	(ANG)	(dB)	Rn/50
2	0.76	25	0.37	0.26
4	0.65	56	0.43	0.22
6	0.51	84	0.48	0.16
8	0.41	118	0.55	0.11
10	0.26	159	0.61	0.08
12	0.26	-144	0.68	0.08
14	0.32	-82	0.89	0.18
16	0.40	-46	1.10	0.29
18	0.40	-26	1.30	0.45
20	0.51	8	1.45	0.55
22	0.41	27	1.69	0.61
24	0.48	75	1.83	0.59
26	0.52	108	2.05	0.40

EXCELICS SEMICONDUCTOR, INC.

Small Signal Equivalent Circuit Model

The small signal model shown below can be useful for extrapolating and interpolating the S-parameters as well as for use in circuit simulators that cannot handle S-parameters directly. The element values are derived by fitting the calculated S-parameters of the model to measured data. The bias points and bonding configuration are as described in the individual device data sheets.



SMALL SIGNAL MODEL

EXCELICS SEMICONDUCTOR, INC.

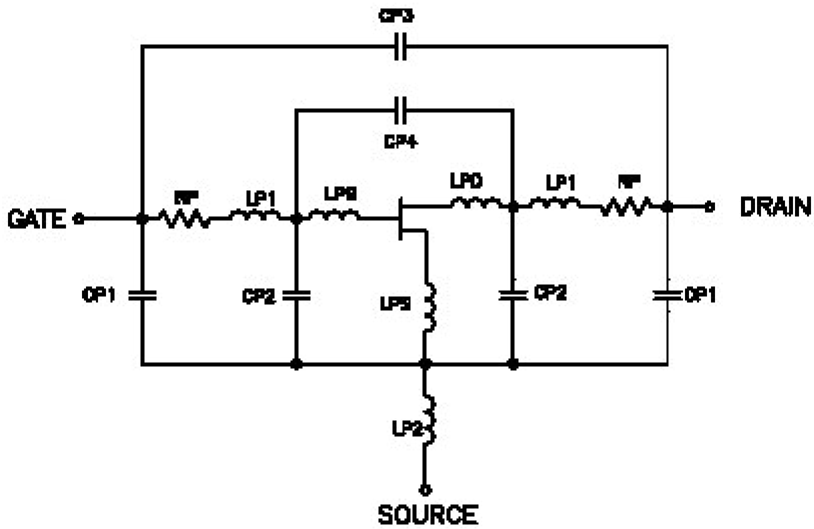
Small Signal Model Element Values
High Efficiency Heterojunction Power FETs

Parameter	L_G	R_G	C_{GS}	R_I	R_S	L_S	C_{GD}	R_{DS}	C_{DS}	R_D	L_D	G_M	τ	C_{PG}	C_{PD}
Units	nH	Ω	pF	Ω	Ω	nH	pF	Ω	pF	Ω	nH	mS	pS	pF	pF
Device:															
EPA018A	0.18	0.50	0.30	0.29	0.13	0.057	0.021	680	0.011	1.0	0.22	55	2.5	0.06	0.06
EPA025A	0.10	1.8	0.33	1.9	0.83	0.071	0.014	280	0.044	1.38	0.18	84	2.0	0.17	0.17
EPA030C	0.20	0.55	0.59	1.6	0.69	0.041	0.024	300	0.025	0.41	0.30	110	2.0	0.084	0.084
EPA040A	0.20	0.74	0.67	1.2	0.52	0.037	0.031	210	0.043	0.55	0.30	140	2.0	0.084	0.084
EPA060A	0.10	0.28	1.2	0.80	0.35	0.028	0.046	120	0.044	0.21	0.15	250	2.0	0.17	0.17
EPA060B	0.20	0.71	1.0	0.80	0.35	0.035	0.044	160	0.064	0.53	0.33	190	2.0	0.084	0.084
EPA080A	0.10	0.37	1.4	0.60	0.26	0.028	0.058	96	0.097	0.28	0.18	260	2.0	0.17	0.17
EPA090A	0.067	0.18	1.6	0.53	0.23	0.022	0.060	73	0.078	0.14	0.089	350	2.0	0.25	0.25
EPA120A	0.067	0.25	1.9	0.40	0.17	0.020	0.085	60	0.16	0.18	0.094	400	2.0	0.25	0.25
EPA120B	0.10	0.35	2.1	0.40	0.17	0.023	0.088	75	0.15	0.26	0.13	380	2.0	0.17	0.17
EPA120E	0.050	0.14	2.1	0.40	0.17	0.018	0.078	52	0.12	0.10	0.045	460	2.0	0.34	0.34
EPA160A	0.050	0.18	2.4	0.30	0.13	0.016	0.11	37	0.26	0.14	0.084	570	2.0	0.34	0.34
EPA160B	0.10	0.47	3.8	0.30	0.13	0.022	0.15	83	0.21	0.35	0.09	810	2.0	0.17	0.17
EPA240B	0.050	0.18	3.3	0.20	0.087	0.050	0.17	27	0.47	0.13	0.074	740	2.0	0.34	0.34
EPA240D	0.28	1.2	4.3	0.20	0.27	0.12	0.14	95	0.30	0.067	0.49	350	4.0	0.25	0.25
EPA480B	0.050	0.35	6.7	0.10	0.043	0.020	0.34	14	0.62	0.26	0.93	1300	2.0	0.37	0.37
EPA480C	0.14	0.61	8.1	0.10	0.13	0.080	0.28	47	0.60	1.1	0.25	670	4.0	0.50	0.50
EPA720A	0.090	0.40	12	0.067	0.090	0.060	0.42	32	0.90	0.70	0.16	1000	4.0	0.76	0.76
EPA960B	0.070	0.31	16	0.050	0.070	0.048	0.56	24	1.2	0.53	0.12	1400	4.0	1.0	1.0
EPA1200A	0.056	0.24	20	0.040	0.050	0.040	0.72	19	1.5	0.42	0.10	1700	4.0	1.3	1.3
High Gain Heterojunction Low Noise FET															
EPB018A	0.22	1.9	0.15	1.6	0.61	0.018	0.040	270	0.015	1.6	0.19	77	2.0	0.08	0.041
EPB025A	0.10	1.8	0.14	1.9	0.83	0.061	0.060	150	0.060	1.4	0.12	78	2.0	0.17	0.17

EXCELICS SEMICONDUCTOR, INC.

Packaged FET Equivalent Circuit Model

Shown below is an approximate model for use with packaged FETs. The FET shown in the schematic can be replaced with the small signal or large signal model for the chip, including bond wire inductances. The element values shown below for the various packages provide a first order approximation, as the exact values will vary depending on the device type.



PACKAGED FET MODEL

Parameter	Units	SOT-89	70 mil	100 mil flange	180 mil flange	CP083
CP1	pF	0.28	0.038	0.05	0.78	0.52
CP2	pF	0.39	0.13	0.2	0.57	0
LP1	nH	1.2	0.25	0.5	0.61	0.56
RP	ohm	0	0.7	0.8	0	0
CP3	pF	0	0.006	0	0	0
CP4	pF	0.3	0	0	0	0
LPG	nH	0	0.3	0.14	0.34	0.06
LPD	nH	0	0.2	0.1	0.2	0.2
LPS	nH	0.009	0.028	0	0.017	0.018
LP2	nH	0	0.065	0.03	0	0

Excelics EPB018A

Curtice-Cubic GaAsFET Model CURTICE3
(Curtice-Ettenberg model)

Parameter	*Description*	*Unit*	*Value*
BETA	Coefficient for pinch-off change with respect to V_{ds}	1/V	0.0511
GAMMA	Hyperbolic tangent function parameter	1/V	1.47
VOUT0	Output voltage (V_{ds}) at which A0, A1, A2, A3 were evaluated	V	2.51
VT0	Value of V1 below which $I_{ds}=I_{ds}(V1=VT0, V_{ds})$	V	-0.9
A0	Cubic polynomial I_{ds} equation coefficent 1	A	0.0524
A1	Cubic polynomial I_{ds} equation coefficent 2	A/V	0.0839
A2	Cubic polynomial I_{ds} equation coefficent 3	A/V^2	0.0257
A3	Cubic polynomial I_{ds} equation coefficent 4	A/V^3	-0.00493
TAU	Transit time under gate	S	2.00E-12
R1	Approximate breakdown resistance	ohm	0
R2	Resistance relating breakdown voltage to channel current	ohm	0
VB0	Gate-drain junction reverse bias breakdown voltage (gate-source junction reverse bias breakdown voltage with $V_{ds}<0$)	V	8
VBI	Built-in gate potential	V	1
RF	Gate-source effective forward-bias resistance	ohm	0
IS	Gate juction reverse saturation current (diode model)	A	1.70E-14
N	Gate junction ideality factor (diode model)	-	1.2
RDS	Additional output resistance for RF operation	ohm	400
CRF	Used with RDS to model frequency dependent output conductance	F	1.00E-08
RD	Drain ohmic resistance	ohm	1
RG	Gate resistance	ohm	0.5
RS	Source ohmic resistance	ohm	1
RIN	Channel resistance	ohm	2.07
CGSO	Zero bias gate-source junction capacitance (diode model)	F	2.60E-13
CGDO	Zero bias gate-drain junction capacitance (diode model)	F	9.00E-14
FC	Coefficient for forward bias depletion capacitance (diode model)	-	0.5
CDS	Drain-source capacitance	F	6.40E-14
CGS	Gate-source capacitance	F	0
CGD	Gate-drain capacitance	F	0
KF4	Flicker noise coefficient	-	0
AF	Flicker noise exponent	-	1
TNOM	Nominal ambiaent temperature at which these model parameters were derived	°C	27
XTI	Temperature exponent for saturation current		3
EG	Energy gap for temperature effect of IS	eV	1.11
VTOTC	VTO temperature coefficent	V/°C	0
BETATCE	Drain current exponential temperature coefficient	%°C	0
FFE	Flicker noise frequency exponent	-	1

7.2. ARCHIVO ".S2P"

```
! VDS=2V  IDS=15MA
# GHZ S MA R 50
! SCATTERING PARAMETERS:
1  .983    -18.6  6.245  162.2 .019    78.9   .53   -13.5
2  .944    -37.5  5.964  144.3 .036    65.2  .507   -28.8
3  .896    -55.5  5.582  127.7 .050    53.6  .485   -42.6
4  .849    -72.6  5.327  112.4 .063    43.6  .464   -54.2
5  .797    -89.2  5.111   97.6 .074    33.1  .421   -65.4
6  .747   -103.7  4.799   83.4 .081    23.4  .370   -78.6
7  .691   -118.6  4.503   69.9 .085    13.9  .344   -90.7
8  .642   -132.8  4.277   57.0 .088     4.7  .303  -100.7
9  .600   -155.6  4.189   42.7 .093    -5.1  .271  -111.2
10 .567   -178.3  4.012   27.8 .096   -16.3  .228  -126.9
11 .534    170.3  3.846   15.5 .094   -26.5  .193  -145.5
12 .515    155.6  3.758    2.9 .093   -33.1  .177  -161.2
13 .555    128.7  3.569  -12.5 .091   -44.2  .137   176.3
14 .596    106.0  3.317  -27.1 .088   -55.6  .114   151.4
15 .592     91.3  3.214  -41.3 .087   -66.9  .141   123.9
16 .597     74.3  3.086  -56.8 .083   -81.1  .158    94.5
17 .619     59.2  2.756  -69.5 .071   -90.3  .134    68.1
18 .670     49.9  2.668  -79.4 .071   -97.3  .136    64.0
19 .668     33.0  2.623  -95.4 .069  -115.9  .169    51.0
20 .708     17.3  2.551 -111.1 .064  -131.4  .172    37.8
21 .757      8.2  2.447 -125.1 .061  -144.1  .159    18.7
22 .743     -2.5  2.325 -139.4 .063  -159.2  .135    14.7
23 .726    -21.1  2.224 -158.5 .065   179.4  .115    -1.3
24 .747    -39.6  2.063 -178.1 .067   158.8  .102   -39.6
25 .709    -52.6  2.024  167.9 .072   144.7  .136   -56.6
26 .683    -70.6  2.006  150.2 .083   132.8  .117   -71.3

! NOISE PARAMETERS:
2  .37   .76   25  .26
4  .43   .65   56  .22
6  .48   .51   84  .16
8  .55   .41  118  .11
10 .61   .26  159  .08
12 .68   .26 -144  .08
14 .89   .32  -82  .18
16 1.1   .40  -46  .29
18 1.3   .40  -26  .45
20 1.45  .51    8  .55
22 1.69  .41   27  .61
24 1.83  .48   75  .59
26 2.05  .52  108  .40
```

BIBLIOGRAFÍA

BIBLIOGRAFÍA

[1] Dambrine, Gilles; Cappy, Alain; Heliodore, Frédéric; Playez, Edouard; *"A new method for determining the FET small-signal equivalent circuit",* IEEE transactions on microwave theory and techniques, vol 36, nº 7, julio 1998.

[2] Berroth, Manfred y Bosch, Roland; *"Broad-band determination of the FET small-signal equivalent circuit",* IEEE transactions on microwave theory and techniques, vol. 38, nº 7, julio 1990.

[3] Golio, J. Michael; "*Microwave MESFETs and HEMTs"*, Boston Artech House, 1991.

[4] Reina Tosina, Javier; Durán Díaz, Iván; Crespo Cárdenas, Carlos; *"Caracterización de circuitos para plataforma de comunicaciones móviles a 5 GHz"*, Actas XVIII Simposium Nacional URSI, Septiembre 2003.

[5] Manual ADS "*Non Linear Devices"*, Agilent Technologies, Mayo 2003.

[6] Manual ADS "*Circuit Simulation"*, Agilent Technologies, Mayo 2003.

[7] Manual ADS "*Introduction to Circuit Componentes"*, Agilent Technologies, Mayo 2003.

[8] Manual ADS *Tuning, Optimization and Statical Design"*, Agilent Technologies, Mayo 2003.

[9] Manual ADS *"Schematic Capture and Layout"*, Agilent Technologies, Mayo 2003.

[10] "*Capítulo IV: Diseño de amplificadores"*, apuntes asignatura de Microondas, Área de Teoría de la Señal del Departamento de Ingeniería Electrónica, Universidad de Sevilla.

[11] Manual ADS *"Amplifier Design Guide"*, Agilent Technologies, Mayo 2003.

[12] Manual ADS *"Expressions, Measurements and Simulation Data Processing"*, Agilent Technologies, Mayo 2003.

[13] *"N9000, PTFE laminates and bolding films"*, Parnelko.

[14] Manual ADS *"LineCalc"*, Agilent Technologies, Mayo 2003.

[15] "*Tema 3: Subsistemas de radio"*, apuntes asignatura de Radiación y Radiocomunicación, Área de Teoría de la Señal del Departamento de Ingeniería Electrónica, Universidad de Sevilla.

[16] Howard, Andy; *"Load-Pull Simulation using ADS"*, presentación de PowerPoint, 28 de mayo del 2002, Agilent Technologies.

[17] Manual ADS *"User-Defined Models: Custom Modelling with Symbolically-Defined Devices"*, Agilent Technologies, Mayo 2003.

[18] Vendelin, George G.; Pavio, Anthony M.; Rohde, Ulrich L.; *"Microwave Circuit Design, using linear and nonlinear techniques"*, Wiley-Interscience, 1990.

[19] Maas, Stephen A.; *"Nonlinear Microwave Circuits"*, Norwood Artech House, 1988.

[20] Manual ADS *"Quick Start: Simulation controllers"*, Agilent Technologies, Mayo 2003.

[21] Anaya de Vega, Enrique; *PFC "Programa APLAC: Análisis de circuitos de microondas"*, Sevilla, Julio 2003.

[22] Galán Martín, Rubén Darío; *PFC "Programa de simulación APLAC: análisis de circuitos no lineales"*, Sevilla, Julio 2003.

[23] Stapleton, Shawn; *"Adaptative digital Predistorsion of power amplifiers",* Agilent Technlogies, Noviembre 2000.

[24] "*Capítulo II: Análisis de Redes de Microondas"*, apuntes asignatura de Microondas, Área de Teoría de la Señal del Departamento de Ingeniería Electrónica, Universidad de Sevilla.

[25] González, G.; *"Design of Amplifiers and Oscillators by the S-parameter Method"*, Prentice Hall, 1984.