CAPITULO 7

ANEXOS

7.1. FUNCIONES DEL PROYECTO

7.1.1. “matriz5.sci”

SciPad - matriz5.sci

File Edit Search Execute Debug Scheme Options Windows Help

```
function M = matriz5(a, N, P)

    b = list(); //Lista para almacenar los vectores retrasados.

//Antes de empezar,
//si el vector de entrada es un vector fila lo transformamos en un vector columna.

    nca = size(a,2);

    if (nca <> 1)
      a = a.';
    end

//Quitamos las N-1 primeras muestras del vector de entrada a y
//construimos los N-1 vectores con retraso.

    i = 1;

    while (N-1 >= i)
      b(N-i) = a;
      i = i+1;
      a(1) = [];
    end

//Ajustamos todos los vectores al mismo tamaño pues
//los vectores resultantes del bucle anterior tienen longitudes diferentes.

    nfa = size (a,1);

    for i = N-1:-1:1

      nfb = size(b(i),1);

      while (nfb > nfa)
        b(i)(nfb) = [];
        nfb = nfb-1;
      end

    end


    m=list(); //Lista que nos servirá para crear la matriz M.
              //La matriz M estará formada por columnas que serán el resultado
              //de ciertas combinaciones de los vectores creados anteriormente.
```

```
    if (modulo(P,2)==0) // Caso P Par.
                        // Se tomará el valor de P impar inmediatamente anterior.

      P=P-1;

    end

//P Impar.
//En cada elemento de la lista se irán almacenando submatrices.
//Cada submatriz en la lista contiene la submatriz anterior. Por ejemplo,
//si en m(1) hemos creado una submatriz de dos columnas m(2) contendrá esas
//dos columnas más las otras que se estimen oportunas.

    n = (P-1)/2;

    //En m(1) se almacena la primera submatriz, cuyo número de columnas
    //solo depende de P.

    m(1) = [a];
    r = a.*a.*conj(a);

    for i = 1: 1: n
      m(1) = [m(1) r]
      r = r.*a.*conj(a);
    end

    //En m(2) se añade una segunda submatriz que sólo dependerá de N.

    m(2) = m(1);

    for i = 1:1:N-1
      m(2) = [m(2) b(i)];
    end

    if(P == 1) //Si P es 1 la función acaba aquí

      M = m(2);

    else // P es impar y distinto de uno
         // Continuamos con la tercera submatriz. El número de columnas dependerá
         //de N y de P.
         // Para la cuarta, quinta y sexta submatriz podemos decir lo mismo.

      m(3) = m(2);
```

```
else // P es impar y distinto de uno
     // Continuamos con la tercera submatriz. El número de columnas dependerá
     //de N y de P.
     // Para la cuarta, quinta y sexta submatriz podemos decir lo mismo.

  m(3) = m(2);

  for k = 1:1:n
    r=(a.*conj(a)).^k

    for i = 1:1:N-1
      m(3) = [m(3) b(i).*r];
    end

  end

  m(4) = m(3);

  for k = 0: 1: n-1
    r=(a.*conj(a))^k

    for i = 1: 1: N-1
      m(4) = [m(4) a.*a.*conj(b(i)).*r];
    end

  end

  m(5) = m(4);

  for k = 0: 1: n-1
    r = (a.*conj(a))^k

    for i = 1:1:N-1
      for j = i:1:N-1
        m(5) = [m(5) conj(a).*b(i).*b(j).*r];
      end
   end

  end

  m(6) = m(5);

  for k=0: 1: n-1
    r=(a.*conj(a))^k
```

```
      for i = 1:1:N-1
        for j = 1:1:N-1
          m(6) = [m(6) a.*b(i).*conj(b(j)).*r];
        end
      end
    end

    if (P < 5) //Aquí acabaría la construción de M en caso de P impar y
               //menor que cinco.
               //Como ya resolvimos el caso P=1, este solo podría ser el caso P=3.

      M = m(6);

    else //Si P es impar y mayor o igual a 5 aparecen nuevas columnas.
         //Añado submatriz con nuevas columnas.

      m(7) = m(6);

      for k = 0: 1: n-2
        r=(a.*conj(a))^k

        for i = 1:1:N-1
          for j = i: 1 :N-1
            m(7) = [m(7) (a.^3).*conj(b(i)).*conj(b(j)).*r];
          end
        end

      end

      M = m(7);//Fin del caso P impar y mayor o igual a cinco

    end
  end


endfunction
```

7.1.2. “NMSE2.sci”

SciPad - NMSE2.sci

File Edit Search Execute Debug Scheme Options Windows Help

```
//Función para comprobar que nuestra funcion matriz funciona correctamente.

function NMSE = NMSE2 (xmed,N,P)

  M = matriz5(xmed,N,P); //Tomo estos dos valores por ejemplo

  ncM = size(M,2);

  t = ones(ncM,1); //Al tomar N=3 y P=3 la matriz M tendrá 15 coumnas
                   //-> t tiene quince elementos

  ymed = M*t;

  //Estimación del modelo

  test = pinv(M)*ymed;

  //Calculo el error cometido MNSE

  ypred = M*test;

  e = ymed - ypred;

  nfe = size(e,1);

  Num = 0;
  for i = 1: 1: nfe
    Num = Num+e(i).*conj(e(i));
  end

  Den = 0;
  for i = 1: 1: nfe
    Den = Den+ymed(i).*conj(ymed(i));
  end

  nmse = Num/Den;
  NMSE = 10*log10(nmse);

endfunction
```

7.1.3.”NMSE3.sci”

SciPad - NMSE3.sci

File Edit Search Execute Debug Scheme Options Windows Help

```
function [NMSE,nftest] = NMSE3 (xs, ys, N, P)

//Estimación del modelo

  M = matriz5 (xs, N, P);

  i = 1;

    while (N-1 >= i) //Quitamos N-1 muestras de ys
      i = i+1;
      ys(1) = [];
    end


  test = pinv(M)* ys;

  nftest = size(test,1);

  //Calculo el error cometido MNSE

  ypred = M * test;

  e = ys - ypred;

  nfe = size(e,1);

  Num = 0;
  for i = 1: 1: nfe
    Num = Num+e(i).*conj(e(i));
  end

  Den = 0;
  for i = 1: 1: nfe
    Den = Den+ys(i).*conj(ys(i));
  end

  nmse = Num/Den;
  NMSE = 10 * log10(nmse);

endfunction
```

7.1.4. "resultados.sci"

SciPad - resultados.sci

File Edit Search Execute Debug Scheme Options Windows Help

```
function [ypred] = resultados (xs, ys, N, P)

//Estimación del modelo. Esta función es idéntica a NMSE3.sci solo que
//me devuelve los resultados predichos por el modelo

  M = matriz5 (xs, N, P);

  i = 1;

    while (N-1 >= i) //Quitamos N-1 muestras de ys
      i = i+1;
      ys(1) = [];
    end


  test = pinv(M)* ys;

  nftest = size(test,1);

  //Calculo el error cometido MNSE

  ypred = M * test;

  e = ys - ypred;

  nfe = size(e,1);

  Num = 0;
  for i = 1: 1: nfe
    Num = Num+e(i).*conj(e(i));
  end

  Den = 0;
  for i = 1: 1: nfe
    Den = Den+ys(i).*conj(ys(i));
  end

  nmse = Num/Den;
  NMSE = 10 * log10(nmse);

endfunction
```

7.1.5. “quitamuestras.sci”

SciPad - quitamuestras.sci

File Edit Search Execute Debug Scheme Options Windows Help

```
//Funcion que me quitará N-1 muestras de una señal cualquiera f

function[f]= quitamuestras (N,f)

i = 1;

    while (N-1 >= i) //Quitamos N-1 muestras de f y la devuelve
      i = i+1;
      f(1) = [];
    end
endfunction
```

7.1.6. “mifft.sci”

SciPad - mifft.sci

File Edit Search Execute Debug Scheme Options Windows Help

```
// Cálculo fft. Resultado en dBm

function y = mifft (f)

  y = fft(f);
  y = fftshift(y);
  y = y.^2/(8*50);
  y = 10*log10(abs(y))+30;

endfunction
```

7.1.7. “coef.sci”

SciPad - coef.sci

File Edit Search Execute Debug Scheme Options Windows Help

```
//Funcion extraida de NMSE3.sci.
//Devolverá sólo el vector de coeficientes del modelo que escojamos

function [test] = coef (xs, ys, N, P)

//Estimación del modelo

  M = matriz5 (xs, N, P);

  i = 1;

    while (N-1 >= i) //Quitamos N-1 muestras de ys
      i = i+1;
      ys(1) = [];
    end


  test = pinv(M)* ys;

endfunction
```

7.2. SEÑALES

7.2.1. Entradas 16-QAM experimental
7.2.2. Salidas 16-QAM experimental
7.2.3. Entrada WCDMA experimental
7.2.4. Salida WCDMA experimental

Ya que no tiene mucho sentido imprimir en papel la ristra de valores de las distintas señales, se ha optado por entregar los ficheros electrónicos. (Ver **CD adjunto**. En este CD se adjuntan todos los anexos en formato electrónico además del presente documento).

7.3. MAX2430

A continuación, se adjunta la hoja de especificaciones proporcionada por el fabricante correspondiente al amplificador MAX2430.

19-1093; Rev 2; 1/98

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

Low-Voltage, Silicon RF Power Amplifier/Predriver

General Description

The MAX2430 is a versatile, silicon RF power amplifier that operates directly from a 3V to 5.5V supply, making it suitable for 3-cell NiCd or 1-cell lithium-ion battery applications. It is designed for use in the 800MHz to 1000MHz frequency range and, at 915MHz, can produce +21dBm (125mW) of output power with greater than 32dB of gain at V_{CC} = 3.6V.

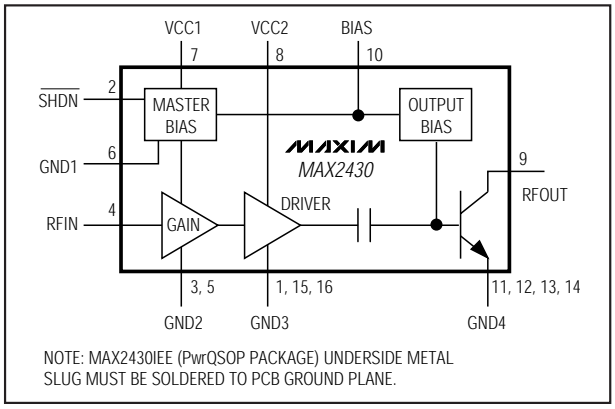
A unique shutdown function provides an off supply current of typically less than 1µA to save power during "idle slots" in time-division multiple-access (TDMA) transmissions. An external capacitor sets the RF output power envelope ramp time. External power control is also possible over a 15dB range. The amplifier's input is matched on-chip to 50Ω. The output is an open collector that is easily matched to a 50Ω load with few external components.

The MAX2430 is ideal as a driver amplifier for portable and mobile telephone systems, or as a complete power amplifier for other low-cost applications, such as those in the 915MHz spread-spectrum ISM band. It is fabricated with Maxim's high-frequency bipolar transistor process and is available in a thermally enhanced, 16-pin narrow SO and miniature 16-pin PwrQSOP packages with heat slug.

Applications

Digital Cordless Phones
915MHz ISM-Band Applications
Two-Way Pagers
Wireless LANs
Cellular Phones
AM and FM Analog Transmitters

Functional Diagram



NOTE: MAX2430IEE (PwrQSOP PACKAGE) UNDERSIDE METAL SLUG MUST BE SOLDERED TO PCB GROUND PLANE.

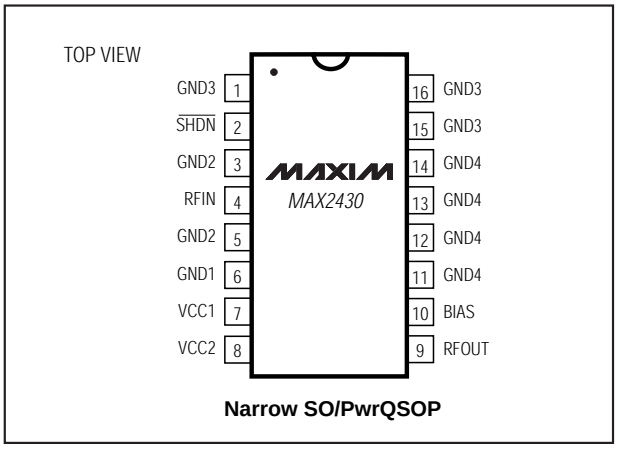
Features

- **Operates Over the 800MHz to 1000MHz Frequency Range**
- **Delivers 125mW at 915MHz from +3.6V Supply (100mW typical from +3.0V supply)**
- **Operates Directly from 3-Cell NiCd or 1-Cell Lithium-Ion Battery**
- **Over 32dB Power Gain**
- **RF Power Envelope Ramping is Programmable with One External Capacitor**
- **Input Matched to 50Ω (VSWR < 2:1)**
- **15dB Output Power Control Range**
- **1µA Typical Shutdown Current**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2430IEE	-20°C to +85°C	16 PwrQSOP
MAX2430ISE	-20°C to +85°C	16 Narrow SO

Pin Configuration



Narrow SO/PwrQSOP

Low-Voltage, Silicon RF Power Amplifier/Predriver

ABSOLUTE MAXIMUM RATINGS

VCC1, VCC2 .....+6V
$\overline{SHDN}$, BIAS.....-0.3V, (V_{CC} + 0.3V)
RFIN.....-0.3V, +2V
P_{RFIN}.....-3dBm
Continuous Power Dissipation (T_A = +70°C)
PwrQSOP (derate 20mW/°C above +70°C).....1.6W
Narrow SO (derate 20mW/°C above +70°C) 1.6W
Operating Temperature Range .....-20°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = VCC1 = VCC2 = RFOUT = 3V to 5.5V, GND1 = GND2 = GND3 = GND4 = 0V, $\overline{SHDN}$ = 2.2V, BIAS = open, RFIN = open, T_A = -20°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}		3		5.5	V
Supply Current	I_{CC}	No RF input applied, V_{CC} = 5.5V		52	70	mA
Shutdown Supply Current	$I_{CC(OFF)}$	$\overline{SHDN}$ = low		1	10	µA
BIAS Pin Voltage	V_{BIAS}	BIAS pin open		2.2		V
$\overline{SHDN}$ High Input	$V_{SHDN(HI)}$		2.2		V_{CC}	V
$\overline{SHDN}$ Low Input	$V_{SHDN(LO)}$				0.4	V
$\overline{SHDN}$ Bias Current	I_{SHDN}	$\overline{SHDN}$ = V_{CC}			18	µA

AC ELECTRICAL CHARACTERISTICS

(MAX2430 EV kit, f = 915MHz, V_{CC} = 3.6V, $\overline{SHDN}$ = V_{CC}, RFOUT matched to 50Ω resistive load, output measurements taken after matching network, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Range		(Note 2)		800		1000	MHz
P_{OUT} at 1dB Compression	P_{1dB}	V_{CC} = 3.6V		20	21.4		dBm
		V_{CC} = 3.0V		19	20.4		
Power Gain	G_P	P_{RFIN} = -20dBm	MAX2430ISE	32	34		dB
			MAX2430IEE	31	33		
Output IM3	OIM3	f1 = 915MHz, f2 = 916MHz, P_{OUT} per tone = 14dBm			-30		dBc
2nd Harmonic		P_{OUT} = P_{1dB}			-26		dBc
3rd Harmonic		P_{OUT} = P_{1dB}			-40		dBc
Efficiency	η	P_{OUT} = P_{1dB}			24		%
Supply Current	I_{CCRF}	P_{OUT} = P_{1dB}			160		mA
Maximum Input VSWR	$VSWR_{IN}$	RFIN connected to 50Ω source			2:1		
Maximum Output Load Mismatch	$VSWR_{OUT}$	V_{CC} = 3V to 5.5V, P_{RFIN} ≤ -10dBm (Note 3)			8:1		
Maximum Output Load Mismatch for Stability	$VSWR_{OUT}$	V_{CC} = 3V to 5.5V, P_{RFIN} ≤ -12dBm (Note 4)			6:1		
Noise Figure	NF				7		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2430 EV kit, f = 915MHz, V_{CC} = 3.6V, $\overline{SHDN}$ = V_{CC}, output matched to 50Ω resistive load, output measurements taken after matching network, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RFIN to RFOUT Isolation		$\overline{SHDN}$ = 0.4V, P_{IN} = -10dBm	MAX2430ISE		50		dB
			MAX2430IEE		47		dB
Turn-On/Off Times		BIAS pin capacitor C1 = 120pF			1		µs
		BIAS pin capacitor C1 = 2.2nF			10		

Note 1: Minimum and maximum parameters are guaranteed by design.

Note 2: For optimum performance at a given frequency, output matching network must be designed for maximum output power. See *Applications Information* section. Operation outside this frequency range is possible but has not been characterized.

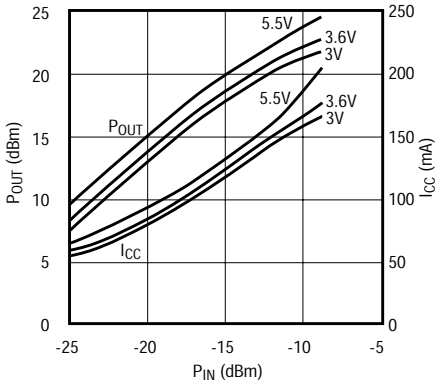
Note 3: No damage to the device.

Note 4: All non-harmonically related outputs are more than 60dB below the desired signal for any electrical phase.

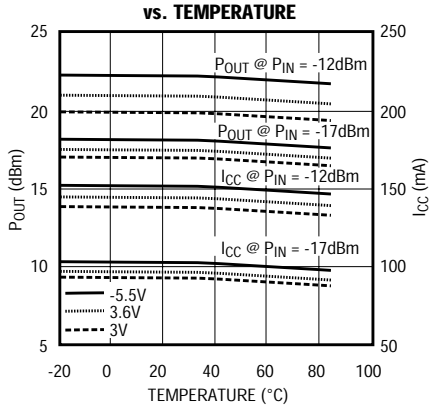
Typical Operating Characteristics

(MAX2430EVKIT-SO, f = 915MHz, V_{CC} = 3.6V, $\overline{SHDN}$ = V_{CC}, output matched to 50Ω resistive load, output measurements taken after matching network, T_A = +25°C, unless otherwise noted.)

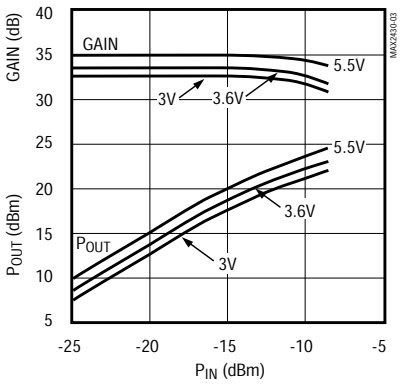
OUTPUT POWER AND CURRENT vs. INPUT POWER



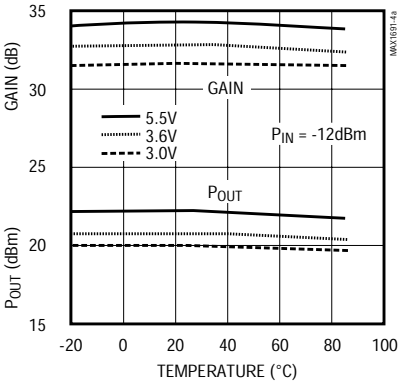
OUTPUT POWER AND CURRENT vs. TEMPERATURE



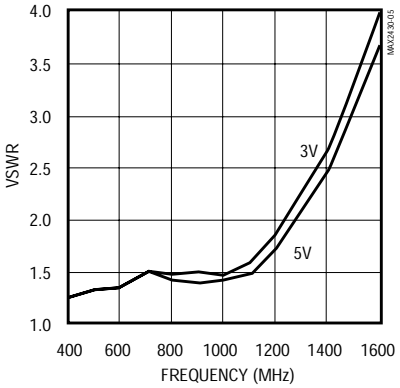
OUTPUT POWER AND GAIN vs. INPUT POWER



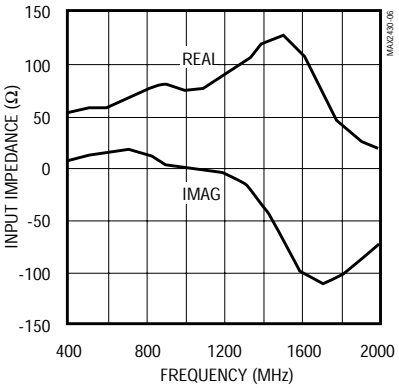
OUTPUT POWER AND GAIN vs. TEMPERATURE (NORMAL OPERATING MODE)



INPUT VSWR vs. FREQUENCY



RF INPUT IMPEDANCE vs. FREQUENCY

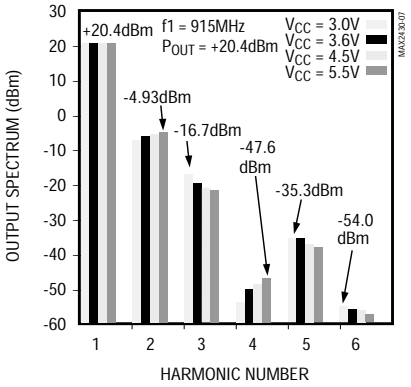


Low-Voltage, Silicon RF Power Amplifier/Predriver

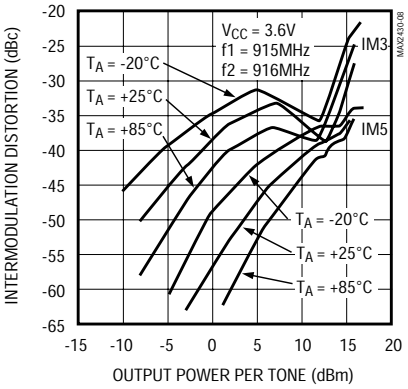
Typical Operating Characteristics (continued)

(MAX2430EVKIT-SO, f = 915MHz, V_{CC} = 3.6V, $\overline{SHDN}$ = V_{CC}, output matched to 50Ω resistive load, output measurements taken after matching network, T_A = +25°C, unless otherwise noted.)

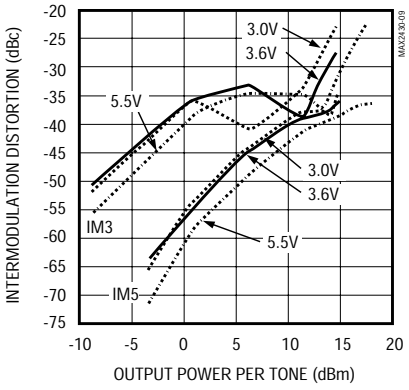
OUTPUT POWER AND HARMONICS



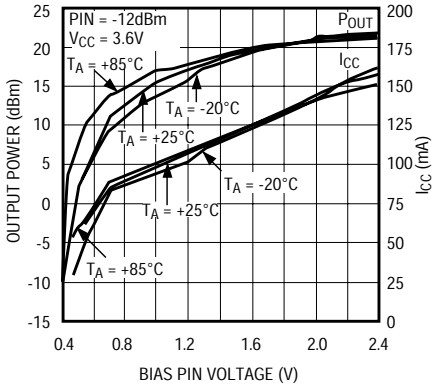
INTERMODULATION DISTORTION vs. OUTPUT POWER AND TEMPERATURE



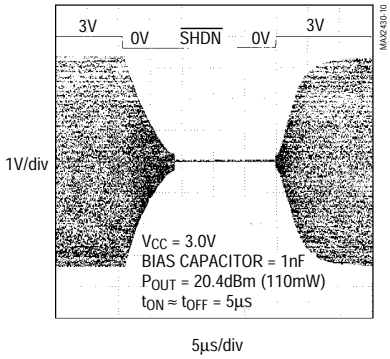
INTERMODULATION DISTORTION vs. OUTPUT POWER AND V_{CC}



OUTPUT POWER AND SUPPLY CURRENT vs. EXTERNAL CONTROL VOLTAGE



RF OUTPUT ENVELOPE CHARACTERISTICS vs. SHUTDOWN CONTROL



Pin Description

PIN	NAME	FUNCTION
1, 15, 16	GND3	Driver Stage Ground. Connect directly to ground plane.
2	$\overline{SHDN}$	Shutdown Input (TTL/CMOS)
3, 5	GND2	Input Stage Ground. Connect directly to ground plane.
4	RFIN	RF Input. Internally matched to 50Ω. Requires series DC-blocking capacitor.
6	GND1	Bias Circuitry Ground. Connect directly to ground plane.
7	VCC1	Bias Circuitry Supply. Connect to supply. Bypass with 1000pF capacitor.
8	VCC2	Driver Stage Output. Connect to supply through inductor (see *Applications Information*).
9	RFOUT	Output Transistor. Open Collector.
10	BIAS	Output Stage Bias Pin. Connect capacitor to GND to control start-up power envelope. Drive directly for power control (see *Applications Information*).
11–14	GND4	Output Stage Ground. Connect directly to ground plane.

Note: *MAX2430IEE (PwrQSOP package) underside metal slug must be soldered to PCB ground plane.*

Detailed Description

The MAX2430 consists of a large power output transistor driven by a capacitively coupled driver stage (see *Functional Diagram*). The driver and front-end gain stages are DC-connected and biased on-chip from the master bias cell. The master bias cell also controls the output stage bias circuit. The input impedance at the RFIN pin is internally matched to 50Ω, while the output stage must be tuned and filtered externally for any narrow-band frequency range of interest between 800MHz and 1000MHz.

The driver amplifier requires an external inductor at the VCC2 pin to provide DC bias and proper matching to the output stage. This inductor's value depends on the package type and frequency range of operation; typically it will vary between 5nH and 22nH.

The output transistor at the RFOUT pin requires an external RF choke inductor connected to the supply for DC bias, and a matching network to transform the desired external load impedance to the optimal internal load impedance of approximately 15Ω.

The MAX2430 includes a unique shutdown feature. The TTL/CMOS-compatible $\overline{SHDN}$ input allows the device to be shut down completely without the use of any external components. Also, the RF output power envelope ramp time can be programmed with a single external capacitor connected between the BIAS pin and ground. Pulling the shutdown pin ($\overline{SHDN}$) high powers on the master bias circuit, which in turn charges the external capacitor tied to the BIAS pin using a controlled current. The voltage at BIAS controls the output power level, which ramps until the BIAS pin is internally clamped to approximately 2.2V. The envelope rampdown time is controlled in a similar manner when the $\overline{SHDN}$ pin is pulled low.

Variable output power control over a 15dB range is also possible by forcing the voltage on the BIAS pin externally from 0.6V to 2.4V.

During the on state ($\overline{SHDN}$ = high), the power-supply bias current is typically 52mA with no RF applied to the input. During the off state ($\overline{SHDN}$ = low), the supply current is typically reduced to less than 1µA.

Low-Voltage, Silicon RF Power Amplifier/Predriver

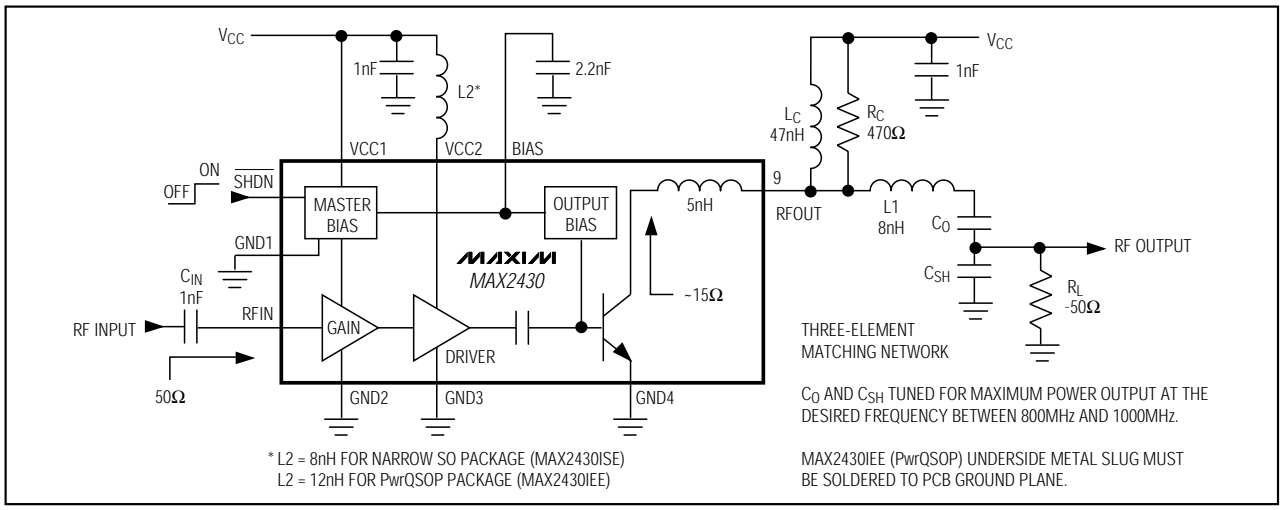


Figure 1. Typical Application Circuit

Applications Information

Output Matching

The optimum internal load impedance seen by RFOUT is approximately 15Ω. This on-chip low drive impedance provides maximum power transfer and best efficiency under low (3V) supply conditions where the voltage-swing headroom is limited. For example, driving an output power of 21.3dBm (135mW) into 50Ω translates to a 7.35Vp-p swing at the output. An RF amplifier would require at least a 4.5V supply to drive a 50Ω load directly. However, driving 21.3dBm into 15Ω translates to 4.02Vp-p. The MAX2430 can achieve a voltage swing of 4.02Vp-p or 2.01Vp from a 3V supply voltage without saturating the output transistor.

Figure 1 shows the MAX2430 configured for 800MHz to 1000MHz operation. The output matching circuitry converts the desired 50Ω load impedance to the 15Ω optimal load seen by the output transistor's collector. This configuration uses a low-loss, controlled-Q inductor network. Starting from the RFOUT pin, this network consists of a series L (which includes the 5nH package parasitic inductance), series C, and shunt C. The design equations for this network are as follows:

R1 = Output resistance as seen by the collector ~15Ω

R_L = Desired load resistance

The controlled-Q inductor network requires that $R_L > R1$ and $Q > \sqrt{(R_L / R1 - 1)}$. Choose Q and compute matching components as given below:

$$\text{Let} \quad A = \sqrt{(R_L \times R1 - R1^2)}$$

$$X_L = Q \times R1$$

$$X_{Co} = X_L - A$$

$$X_{Csh} = R_L \times R1 / A$$

$$L1 = X_L / \omega - 5\text{nH of package inductance}$$

$$C_O = \frac{1}{\omega X_{Co}}$$

$$C_{SH} = \frac{1}{\omega X_{Csh}}$$

where ω equals the center frequency in radians/second.

Recommended starting values for L1 and L2 are given in Table 1.

Table 1. Recommended L1 and L2 Starting Values

f = ω / 2π (MHz)	L1(nH)	MAX2430ISE L2(nH)	MAX2430IEE L2(nH)
400 to 600*	22	12	18
600 to 800*	15	8	12
800 to 1000	8	8	12

*Not characterized

An overall loaded Q ≤ 5 can be achieved with readily available surface-mount components. This network absorbs the parasitic elements of the surface-mount components in such a way that they do not negatively impact the stopband characteristics; in fact, they can improve the overall stopband attenuation with properly chosen components. High-Q components (Q > 100) that have self-resonance near the 3rd harmonic of the intended output frequency should provide good passband characteristics with low loss, while offering good attenuation of the undesired 2nd and 3rd harmonics that are generated. Note that most applications will require extra filtering components and good shielding after the matching network to ensure absolute attenuation of out-of-band signals in order to meet out-of-band spurious suppression requirements.

Output Mismatch Considerations

The MAX2430 will typically withstand an output load mismatch of VSWR = 6:1 at any electrical phase without exhibiting oscillatory behavior over the entire supply voltage range of 3V to 5.5V. Resistor R_C enhances stability under load mismatch conditions and does not affect normal operation of the circuit.

BIAS Pin

The voltage at the BIAS pin controls the output power transistor biasing. At BIAS = 0.6V, the output transistor is biased to Class C, resulting in low gain and relatively nonlinear power. Above 2V, the output stage is biased to Class AB. Note that changing the bias voltage may degrade the output transistor's stability.

The shutdown pin ($\overline{SHDN}$) controls the master bias circuit, which in turn provides a control current of approximately 500 A to the external capacitor connected to the BIAS pin. When $\overline{SHDN}$ transitions from low to high, the BIAS pin capacitor charges up and clamps at approximately 2.2V. When $\overline{SHDN}$ transitions from high to low, the BIAS pin capacitor is discharged to nearly ground. This results in a power-up/power-down ramping of the RF envelope, which can be approximated by the following equation:

$$t_{ramp} \cong C_{BIAS} \times 2.2V / 0.5mA = 4400\Omega \times C_{BIAS}$$

Therefore, a 2.2nF capacitor will give approximately 10 s ramp time.

The BIAS pin can also be used to control the final output power and gain over a 15dB range, by forcing the BIAS pin voltage externally between 0.6V and 2.4V. Note that the BIAS pin driver must be able to source/sink 700 A. Forcing the BIAS pin directly in this manner disrupts the RF envelope timing function. To avoid this, place a diode in series with the BIAS pin control circuit, as shown in Figure 2.

Note that when using the BIAS pin for power control, linearity is much degraded at the lower power levels.

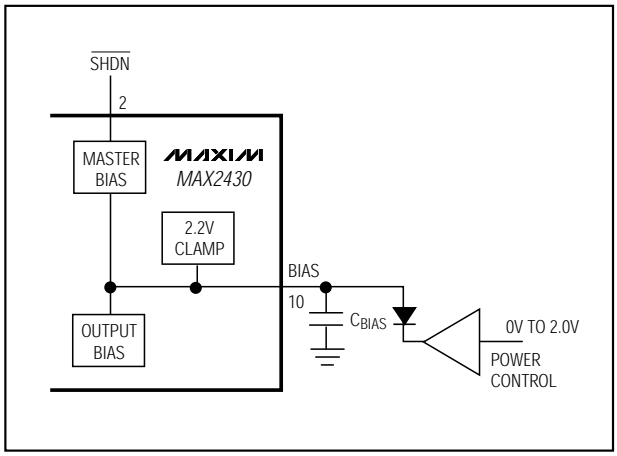


Figure 2. Power-Control Application Using BIAS Pin

Operating Frequency Range

The MAX2430 has been characterized for operation in the 800MHz to 1000MHz range. Operation outside this range is possible, but the following issues must be considered:

- Gain increases substantially at lower frequencies, possibly causing stability problems.
- Useful gain and output power levels drop rapidly above 1000MHz.

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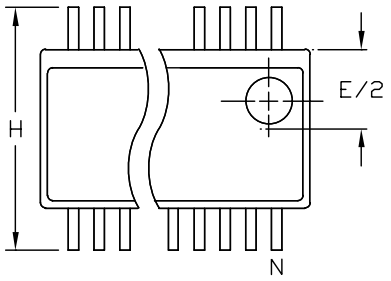
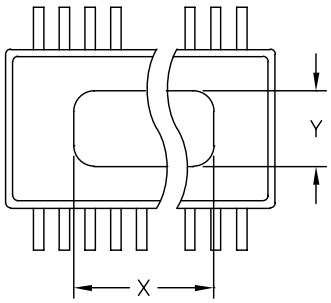
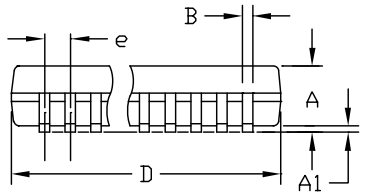
Package Information

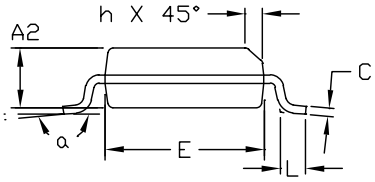
PSSOPPS.EPS





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.010	0.127	0.25
A2	.055	.059	1.40	1.55
B	.008	.012	0.20	0.31
C	.007	.010	0.19	0.25
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°





VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
X	.107	.123	2.717	3.124		

D	.386	.391	9.80	9.98	28	AB
X	.271	.287	6.883	7.290		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006"
3. CONTROLLING DIMENSIONS: INCHES

MAXIM
PROPRIETARY INFORMATION

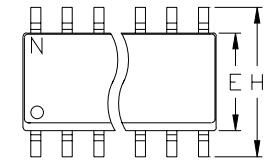
TITLE:
PACKAGE OUTLINE, POWER QSOP (PSSOP2)

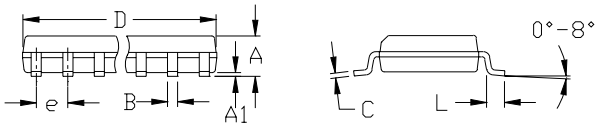
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0063	A	1/1

Low-Voltage, Silicon RF Power Amplifier/Predriver

Package Information (continued)

SOICEPS





	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .150" (TITLE) | 1/1 | 21-0041 A (DOCUMENT CONTROL NUMBER / REV.)

NOTES